

Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG ,CPU-Memory	3,4
CPU-Power ,CPU-GND	5,6
DDRIII DIMMA1&DDRIII DIMMB1	7,8
LYNX-PCI /E/DMI /USB/CLK	9
LYNX-SATA/HOST/FAN/GPIO/VGA	10
LYNX-SMB/LPC/AUDIO/RTC/RST	11
LYNX-POWER PIN,GND/ LYNX STRAPS	12,13 ,14
PCIE1(X1) & PCIE2(X16) Slots	15
DVI , HDMI	16,17
SIO-NUVOTON NCT6779D	18
ALC892/887	19
LAN RTL8111G/8106E	20
SATA /USB3.0 Connector	21
USB3.0 Renes UPD720202 2PORT	22
USB2.0 Connector	23
VGA	24
ACPI Controller UPI	25
CPU Power - ISL95812,CPU Power - MOS	26 27
DDR Power -UP1513 1-Phase	28
PCH Power - OP+MOS	29
PCH Power - ME Power	30
FAN	31
ATX F_Panel/EMI /TPM/LPT	32
XDP CPU & COM PORT	33
Manual Parts	34

MS-7846 *mATX*

Ver: 2.1

Intel Sharkbay platform H81 COLAY B85 H87

CPU:

INTEL-Haswell LGA1150

System Chipset:

H81,B85,H87

Memory:

*DDRIII (1333/1666MHz) * 2 (Dual Channel)*

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL887

LAN-realtek8111G

SIO:NUVOTON 6779D

SPI ROM: 64 MB & 128MB

Expansion Slots:

*PCI Express (X16) Slot * 1*

*PCI Express (X1) Slot * 2*

Other:

*VGA*1*

*SATA2*2*

*SATA3*2*

*FRONT USB2.0 *4*

*FRONT USB3.0 *2*

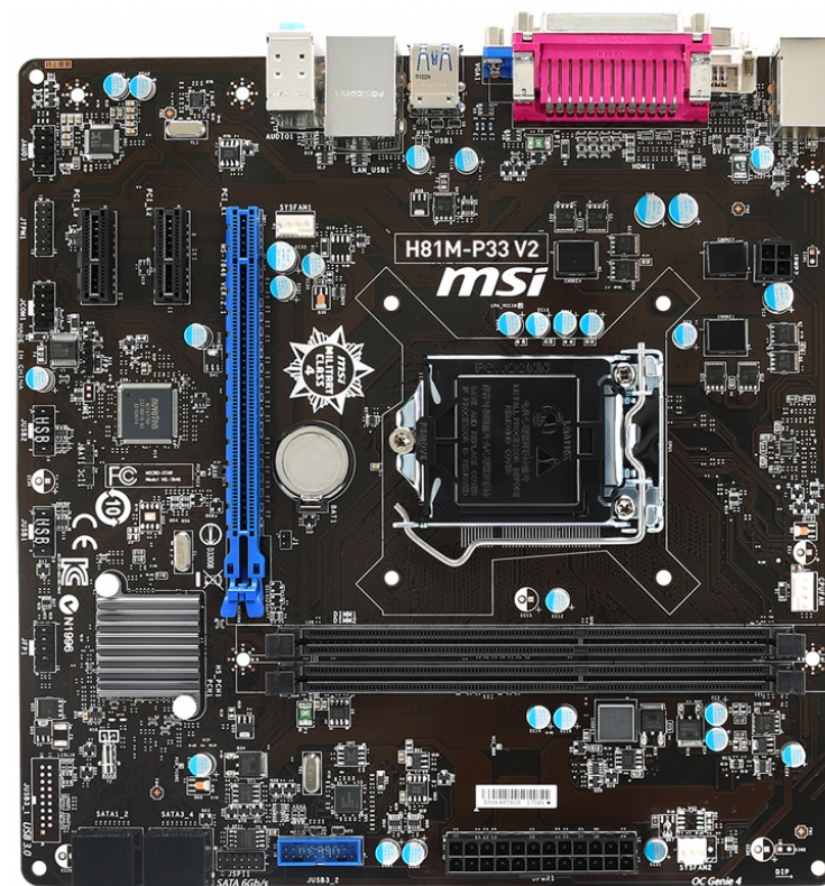
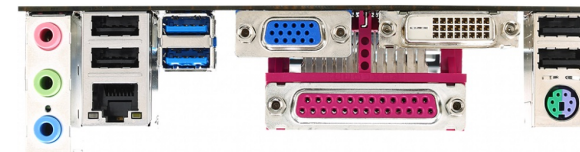
*REAL USB2.0 *2*


*REAL USB3.0 *2*

*PS2*1*

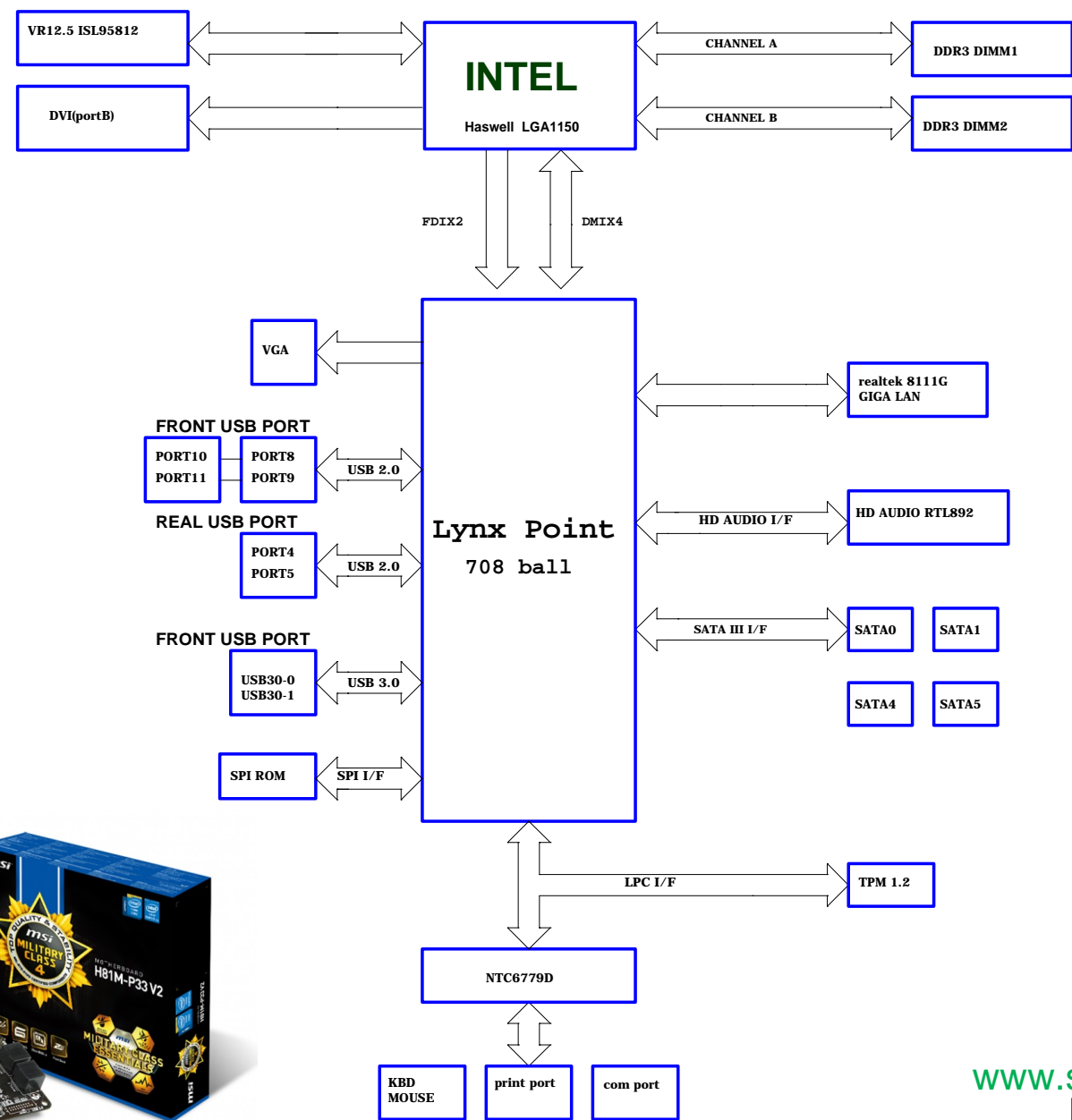
*FRONT COM PORT*1*

*REAL PRINT PORT*1*



			MICRO-STAR INT'L CO.,LTD	
			MS-7846	
Size	Document Description	Rev		
Custom	Cover Sheet	2.1		
Date: Monday, August 12, 2013		Sheet 1 of 38		

MS-7846 Block Diagram



www.schematic-x.blogspot.com

CPU1G

7 OF 9

- A13 VSS_001
- A15 VSS_002
- A17 VSS_003
- A23 VSS_004
- A11 VSS_005
- AA3 VSS_006
- AA33 VSS_007
- AA36 VSS_008
- AA38 VSS_009
- AA6 VSS_010
- AA7 VSS_011
- AA8 VSS_012
- A5 VSS_013
- AB34 VSS_014
- AB37 VSS_015
- AB5 VSS_016
- AB7 VSS_017
- AC3 VSS_018
- AC33 VSS_019
- AC34 VSS_020
- AC36 VSS_021
- AC36 VSS_022
- AC37 VSS_023
- AC38 VSS_024
- AC39 VSS_025
- AC40 VSS_026
- AC6 VSS_027
- AC7 VSS_028
- A7 VSS_029
- AD1 VSS_030
- AD2 VSS_031
- AD3 VSS_032
- AD33 VSS_033
- AD36 VSS_034
- AD4 VSS_035
- AD6 VSS_036
- AD6 VSS_037
- AD7 VSS_038
- AD8 VSS_039
- AE33 VSS_040
- AE36 VSS_041
- AE37 VSS_042
- AE40 VSS_043
- AE5 VSS_044
- AE8 VSS_045
- AF1 VSS_046
- AF33 VSS_047
- AF36 VSS_048
- AF4 VSS_049
- AF5 VSS_050
- AF8 VSS_051
- AG33 VSS_052
- AG36 VSS_053
- AG37 VSS_054
- AG38 VSS_055
- AG39 VSS_056
- AG40 VSS_057
- AG5 VSS_058
- AG8 VSS_059
- AH1 VSS_060
- AH2 VSS_061
- AH3 VSS_062
- AH33 VSS_063
- AH36 VSS_064
- AH4 VSS_065
- AH5 VSS_066
- AH8 VSS_067
- AJ11 VSS_068
- AJ14 VSS_069
- AJ16 VSS_070
- AJ18 VSS_071
- AJ19 VSS_072
- AJ22 VSS_073
- AJ23 VSS_074
- AJ26 VSS_075
- AJ27 VSS_076
- AJ30 VSS_077
- AJ31 VSS_078
- AJ32 VSS_079
- AJ33 VSS_080
- AJ34 VSS_081
- AJ35 VSS_082
- AJ36 VSS_083
- AJ37 VSS_084
- AJ40 VSS_085
- AJ5 VSS_086
- AJ8 VSS_087
- AK1 VSS_088
- AK10 VSS_089
- AK11 VSS_090

HASWELL

- AK12 VSS_091
- AK13 VSS_092
- AK14 VSS_093
- AK19 VSS_094
- AK24 VSS_095
- AK25 VSS_096
- AK26 VSS_097
- AK27 VSS_098
- AK28 VSS_099
- AK29 VSS_100
- AK30 VSS_101
- AK36 VSS_102
- AK4 VSS_103
- AK5 VSS_104
- AK6 VSS_105
- AK7 VSS_106
- AK8 VSS_107
- AK9 VSS_108
- AL3 VSS_109
- AL4 VSS_110
- AL17 VSS_111
- AL21 VSS_112
- AL24 VSS_113
- AL27 VSS_114
- AL36 VSS_115
- AL37 VSS_116
- AL38 VSS_117
- AL39 VSS_118
- AL40 VSS_119
- AL5 VSS_120
- AL6 VSS_121
- AL7 VSS_122
- AM1 VSS_123
- AM11 VSS_124
- AM12 VSS_125
- AM13 VSS_126
- AM14 VSS_127
- AM15 VSS_128
- AM19 VSS_129
- AM2 VSS_130
- AM27 VSS_131
- AM3 VSS_132
- AM31 VSS_133
- AM32 VSS_134
- AM33 VSS_135
- AM34 VSS_136
- AM35 VSS_137
- AM36 VSS_138
- AM37 VSS_139
- AM4 VSS_140
- AM4 VSS_141
- AN10 VSS_142
- AN11 VSS_143
- AN14 VSS_144
- AN18 VSS_145
- AN2 VSS_146
- AN22 VSS_147
- AN24 VSS_148
- AN24 VSS_149
- AN24 VSS_150
- AN24 VSS_151
- AN36 VSS_152
- AN37 VSS_153
- AN37 VSS_154
- AN40 VSS_155
- AN6 VSS_156
- AN7 VSS_157
- AN8 VSS_158
- AN8 VSS_159
- AP1 VSS_160
- AP11 VSS_161
- AP14 VSS_162
- AP24 VSS_163
- AP24 VSS_164
- AP27 VSS_165
- AP27 VSS_166
- AP4 VSS_167
- AP4 VSS_168
- AP5 VSS_169
- AP5 VSS_170
- AR11 VSS_171
- AR16 VSS_172
- AR17 VSS_173
- AR18 VSS_174
- AR18 VSS_175
- AR20 VSS_176
- AR21 VSS_177
- AR22 VSS_178
- AR22 VSS_179
- AR22 VSS_180

GND

CPU1H

8 OF 9

- J6 VSS_361
- K1 VSS_362
- K18 VSS_363
- K20 VSS_364
- K22 VSS_365
- K24 VSS_366
- K26 VSS_367
- K28 VSS_368
- K30 VSS_369
- K34 VSS_370
- K36 VSS_371
- K4 VSS_372
- K40 VSS_373
- K7 VSS_374
- L7 VSS_375
- L8 VSS_376
- L9 VSS_377
- C4 VSS_378
- B4 VSS_379
- B4 VSS_380
- B36 VSS_381
- B34 VSS_382
- B38 VSS_383
- B28 VSS_384
- B26 VSS_385
- B24 VSS_386
- A77 VSS_387
- A5 VSS_388
- A5 VSS_389
- A27 VSS_390
- A26 VSS_391
- A23 VSS_392
- A26 VSS_393
- A26 VSS_394
- M28 VSS_395
- M30 VSS_396
- M32 VSS_397
- M34 VSS_398
- M3 VSS_399
- M4 VSS_400
- M40 VSS_401
- M5 VSS_402
- M6 VSS_403
- M7 VSS_404
- K15 VSS_405
- K16 VSS_406
- N1 VSS_407
- N2 VSS_408
- N3 VSS_409
- N7 VSS_410
- N4 VSS_411
- N4 VSS_412
- N6 VSS_413
- K32 VSS_414
- P2 VSS_415
- P34 VSS_416
- P38 VSS_417
- P5 VSS_418
- P7 VSS_419
- N8 VSS_420
- R3 VSS_421
- L36 VSS_422
- R35 VSS_423
- R40 VSS_424
- R5 VSS_425
- R6 VSS_426
- R7 VSS_427
- T1 VSS_428
- T2 VSS_429
- T33 VSS_430
- T39 VSS_431
- T4 VSS_432
- T4 VSS_433
- T5 VSS_434
- T6 VSS_435
- T7 VSS_436
- R8 VSS_437
- U2 VSS_438
- U33 VSS_439
- U34 VSS_440
- U37 VSS_441
- U4 VSS_442
- U7 VSS_443
- P35 VSS_444
- V3 VSS_445
- V33 VSS_446
- V40 VSS_447
- V6 VSS_448
- V8 VSS_449
- W1 VSS_450
- W33 VSS_451
- W35 VSS_452
- W37 VSS_453
- W4 VSS_454
- W7 VSS_455
- Y33 VSS_456
- Y4 VSS_457
- Y5 VSS_458
- Y6 VSS_459

GND

- MEC1 MEC1
- MEC2 MEC2
- MEC3 MEC3
- MEC4 MEC4
- MEC5 MEC5
- MEC6 MEC6
- MEC7 MEC7

VSS1 R148 X OR

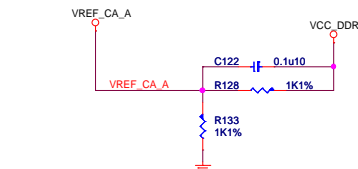
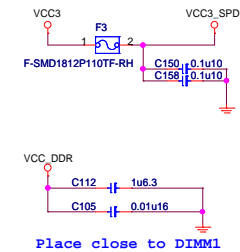
VSS2 R147 X OR



MICRO-STAR INT'L CO.,LTD

MS-7846

Size Custom	Document Description CPU-GND	Rev 2.1
Date: Monday, August 12, 2013	Sheet 6 of 38	



DDRIII-240P_BLACK-RH-24



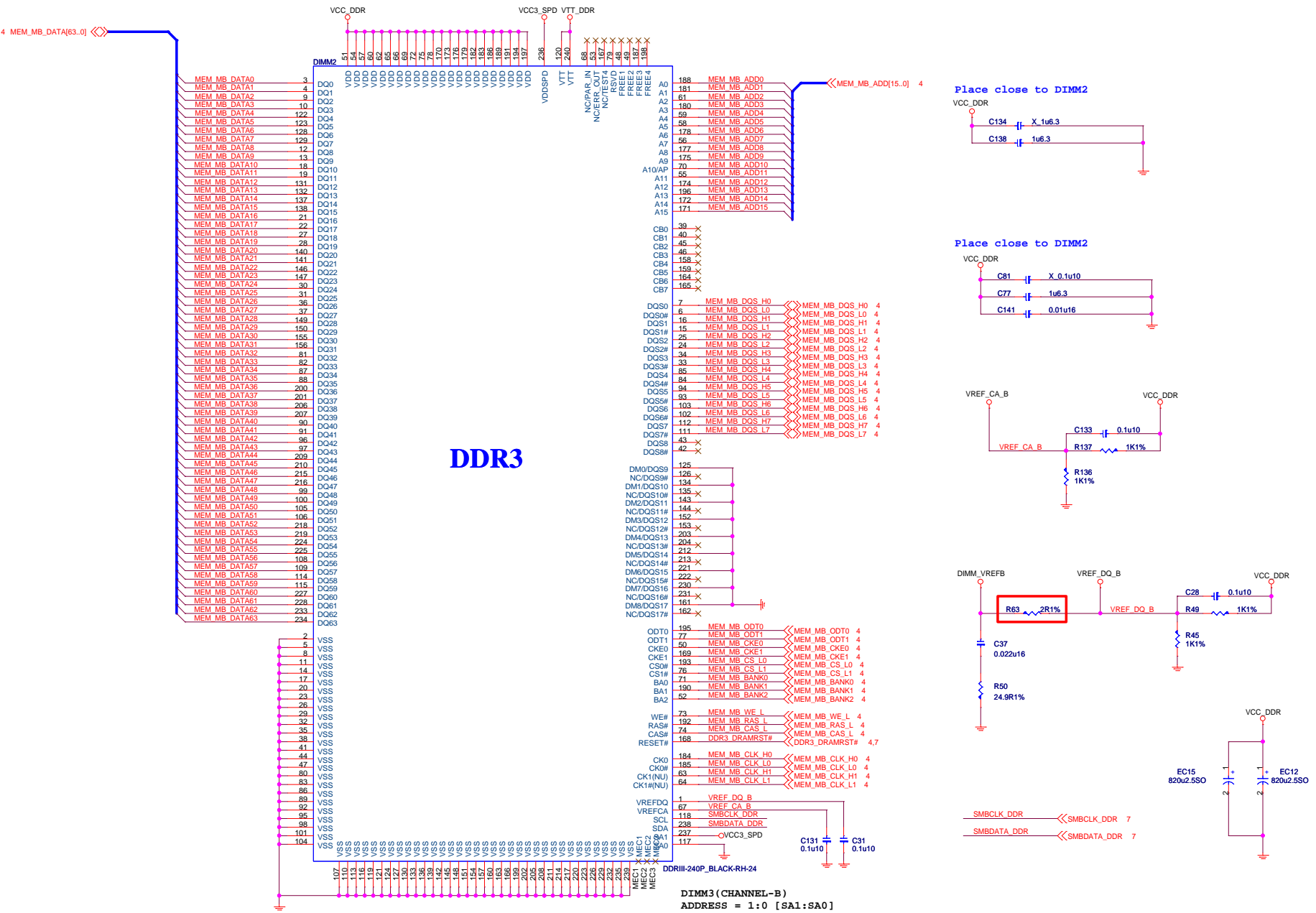
MICRO-STAR INT'L CO.,LTD

MS-7846

Size Custom	Document Description DDR3 Chanel-A DIMM1/2	Rev 2.1
Date: Monday, August 12, 2013		Sheet 7 of 38


DDRIII DIMM_B0

DDR3

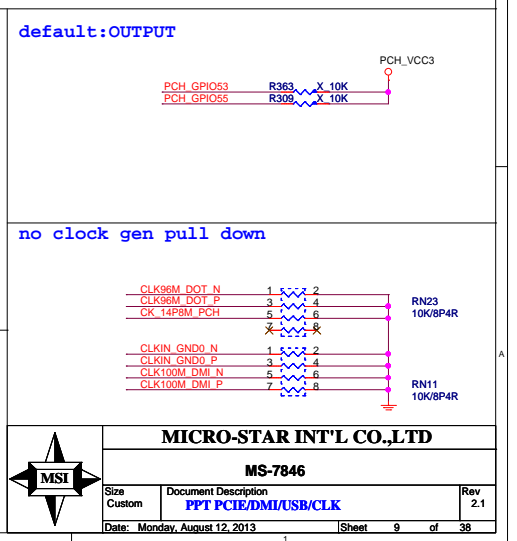
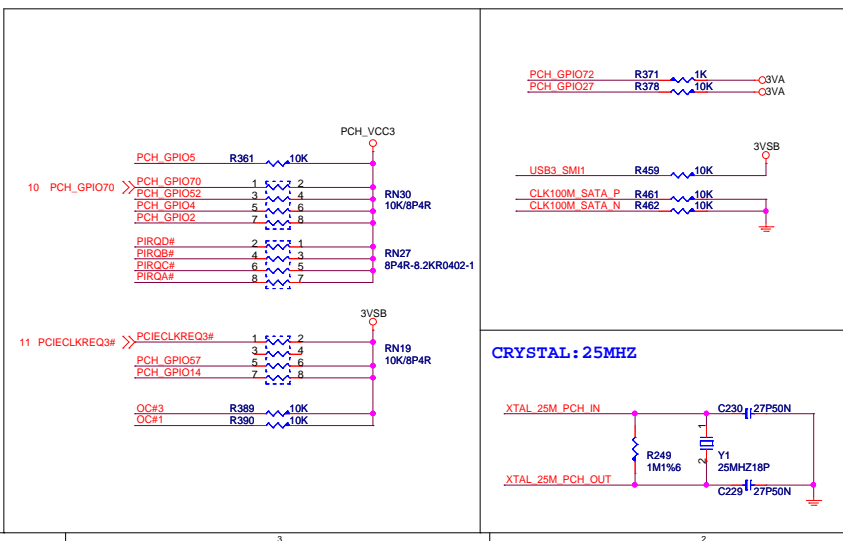
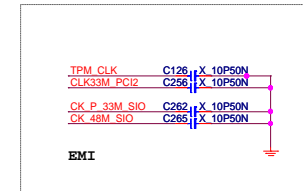


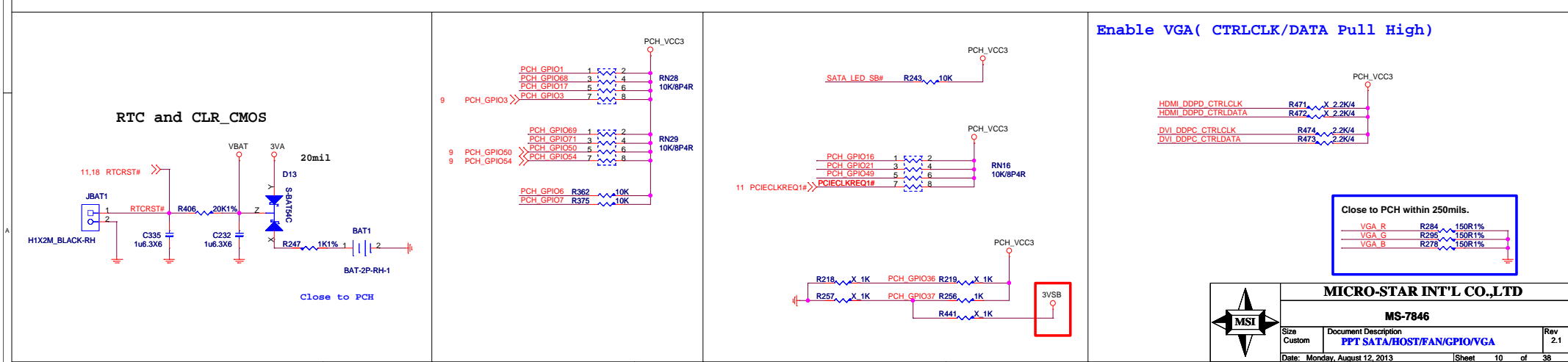
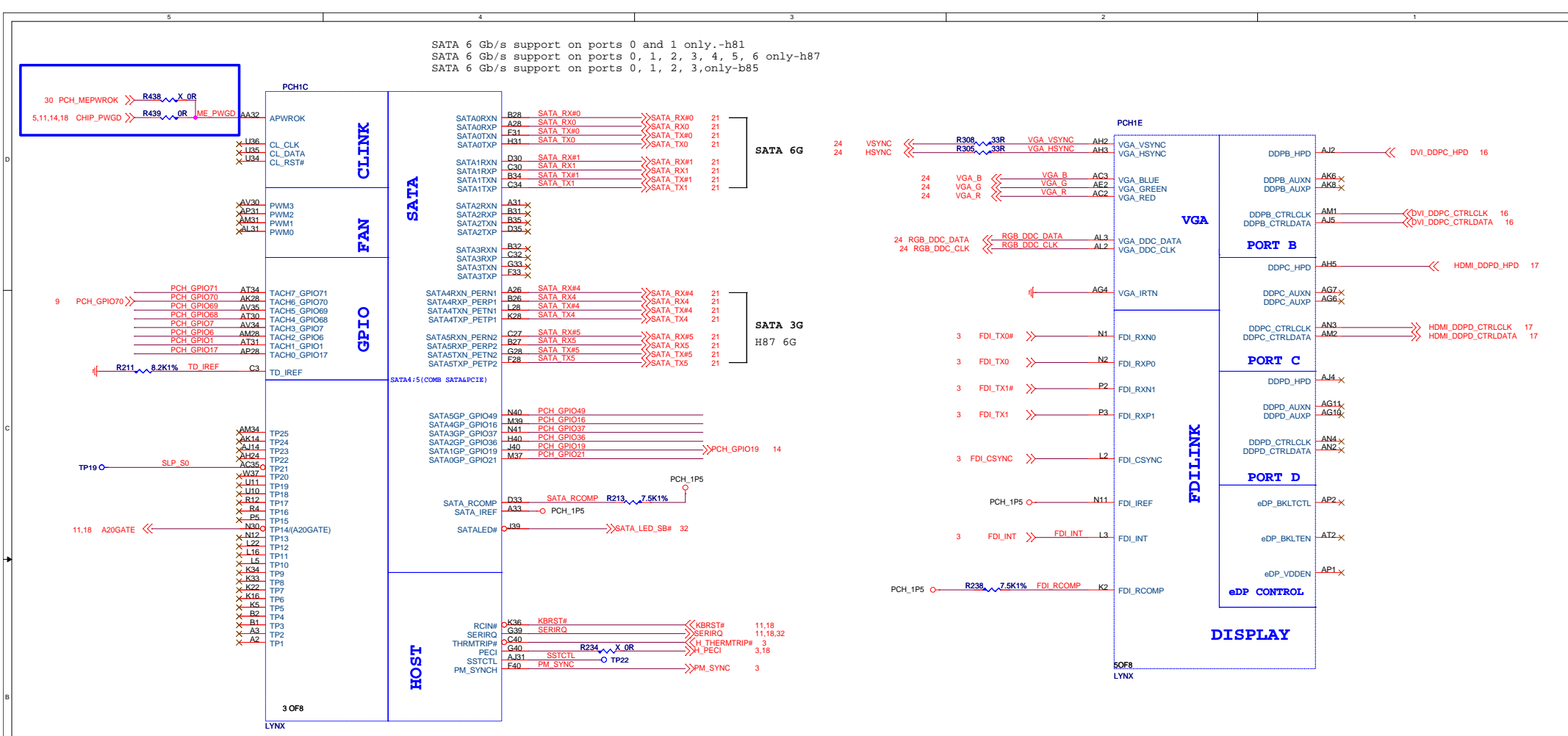
Place close to DIMM2

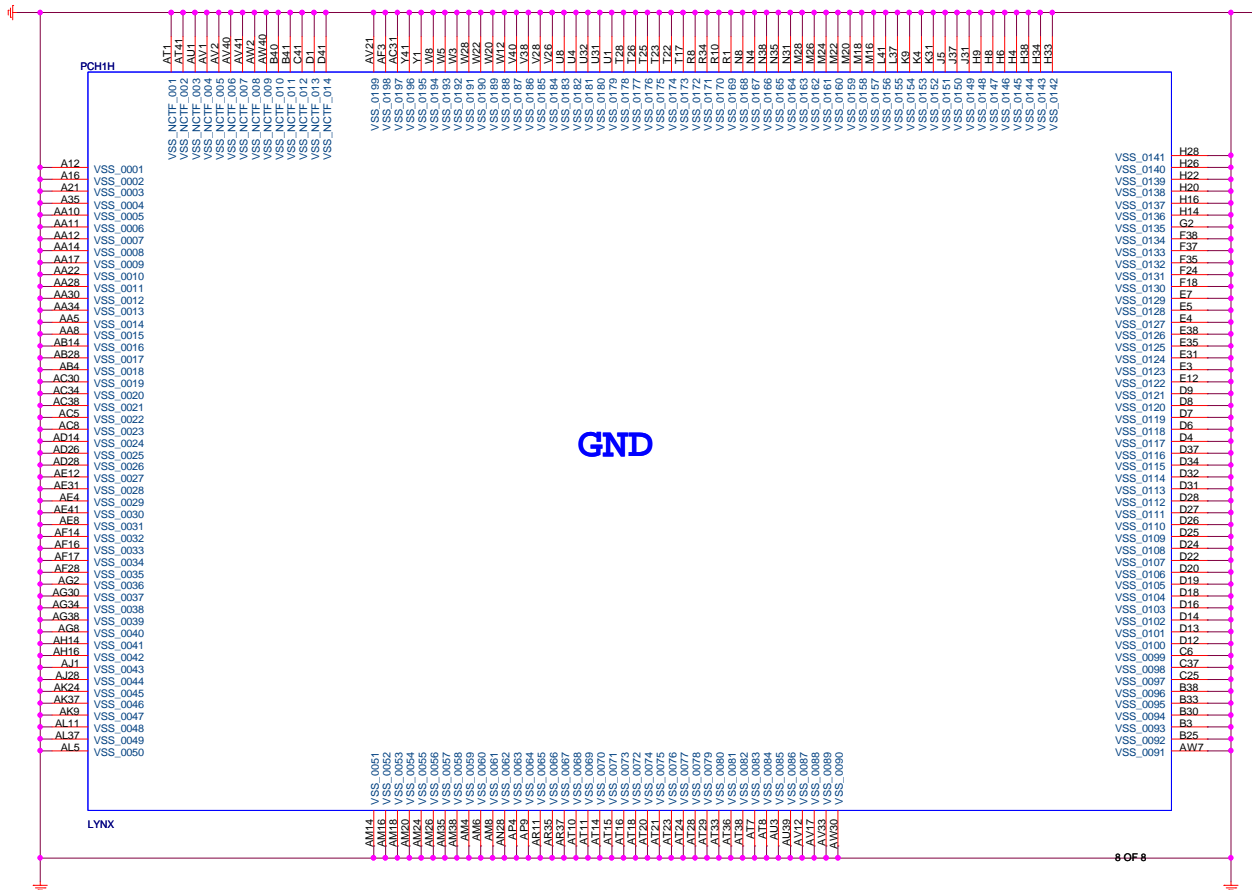
Place close to DIMM2



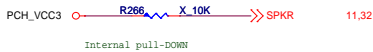
MICRO-STAR INT'L CO.,LTD		
MS-7846		
Size Custom	Document Description DDR3 ChaneL-B DIMM3/4	Rev 2.1
Date: Monday, August 12, 2013		Sheet 8 of 38

[illegible]





PCH Straps



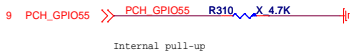
SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:

Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



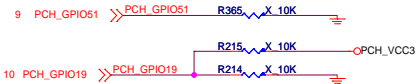
GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:

Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GP/GPIO19, GPIO51

Default (SPI):

Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required.

Boot from PCI:

Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.

Leave GPIO51 Floating.

Boot from LPC:

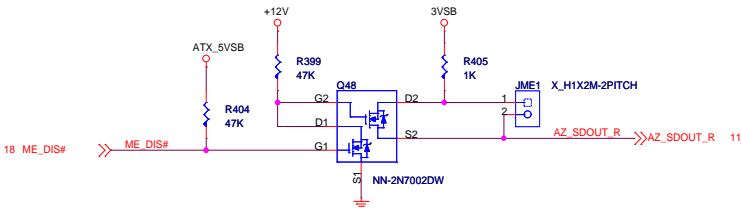
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.

Connect to ground with 1k Ohm pull-down resistor.



HDA_SDO

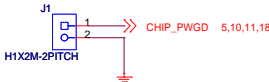
Default:

Do not pull high.

Disable ME in Manufacturing Mode:

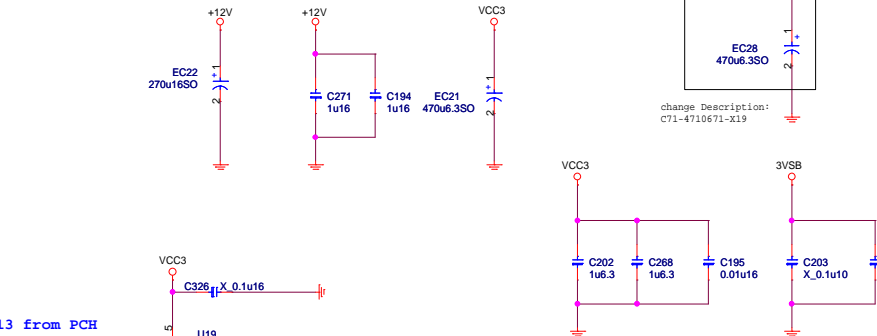
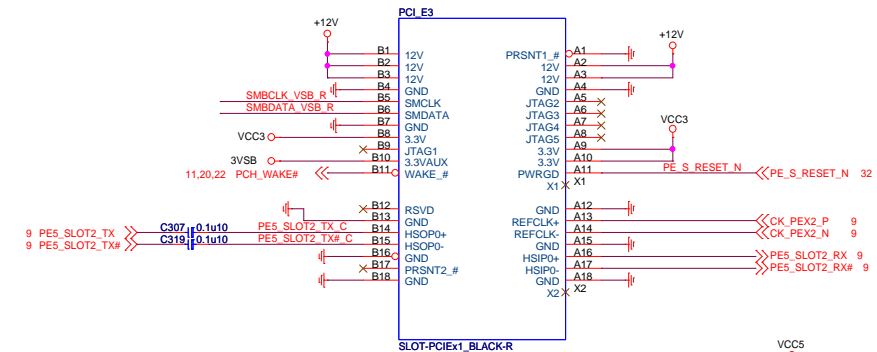
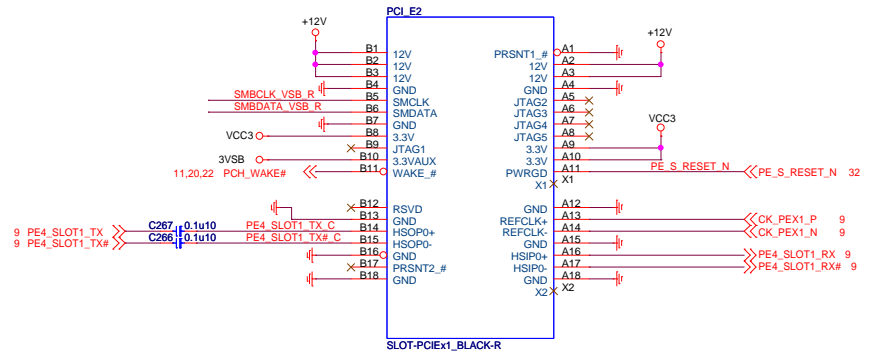
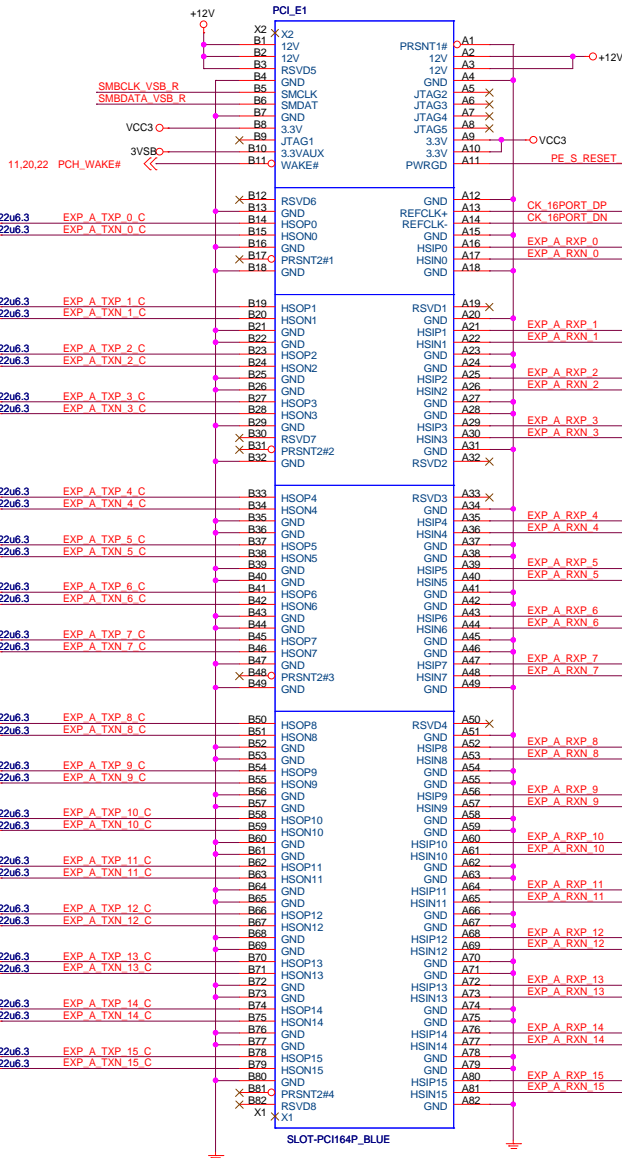
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

For test cpu voltage



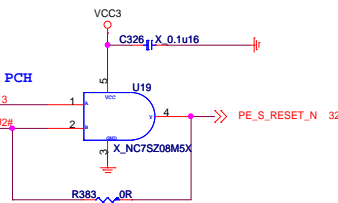
11 SMBCLK_VSB_R
11 SMBDATA_VSB_R

SMBCLK_VSB_R
SMBDATA_VSB_R



GPIO13 from PCH

11 PCH_GPIO13 >> PCH_GPIO13
18 PLTRST_BU2# >> PLTRST_BU2#
PCIE_SLOT_RESET_N
from SIO RESET_BUS2



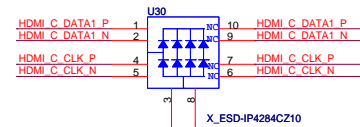
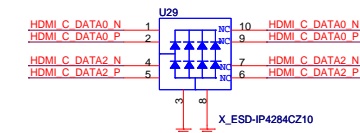
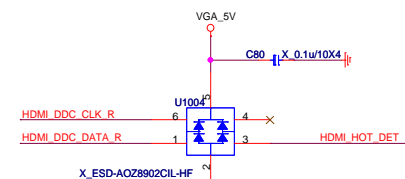
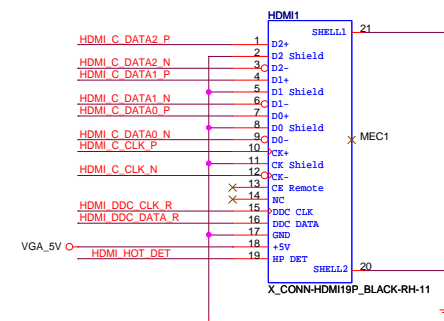
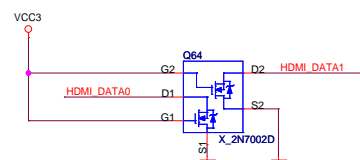
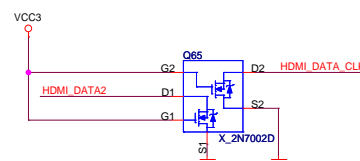
MICRO-STAR INT'L CO.,LTD

MS-7846

Size	Document Description	Rev
Custom	PCIE1(X1) & PCIE2(X16) Slots	2.1
Date:	Monday, August 12, 2013	Sheet 15 of 38

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

3	HDMI_DDPD_CLK_P	C255	X 0.1u10X4	HDMI_C_CLK_P	R360	X 470R1%0402	
3	HDMI_DDPD_CLK_N	C270	X 0.1u10X4	HDMI_C_CLK_N	R359	X 470R1%0402	
3	HDMI_DDPD_CLK_N	C272	X 0.1u10X4	HDMI_C_DATA2_P	R380	X 470R1%0402	HDMI_DATA_CLK
3	HDMI_DDPD_TX2_P	C263	X 0.1u10X4	HDMI_C_DATA2_N	R384	X 470R1%0402	HDMI_DATA2
3	HDMI_DDPD_TX2_N	C269	X 0.1u10X4	HDMI_C_DATA1_P	R392	X 470R1%0402	
3	HDMI_DDPD_TX1_P	C261	X 0.1u10X4	HDMI_C_DATA1_N	R388	X 470R1%0402	HDMI_DATA1
3	HDMI_DDPD_TX1_N	C250	X 0.1u10X4	HDMI_C_DATA0_P	R379	X 470R1%0402	
3	HDMI_DDPD_TX0_P	C257	X 0.1u10X4	HDMI_C_DATA0_N	R391	X 470R1%0402	HDMI_DATA0



HDMI C. CLK N

HDMI C. CLK P

R460
X_180R/1%4

HDMI C. DATA0 N

HDMI C. DATA0 P

R468
X_180R/1%4

HDMI C. DATA1 N

HDMI C. DATA1 P

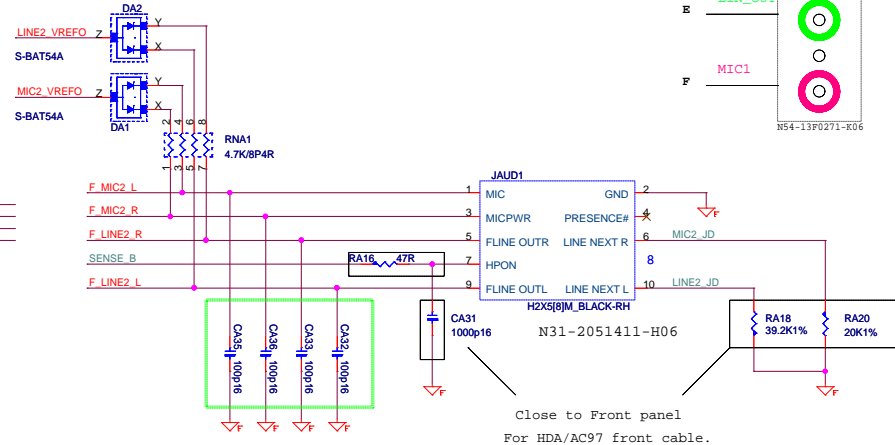
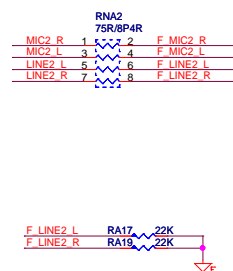
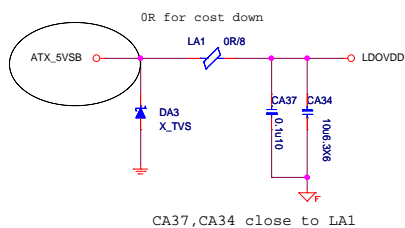
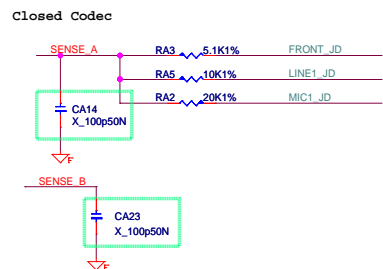
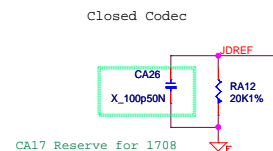
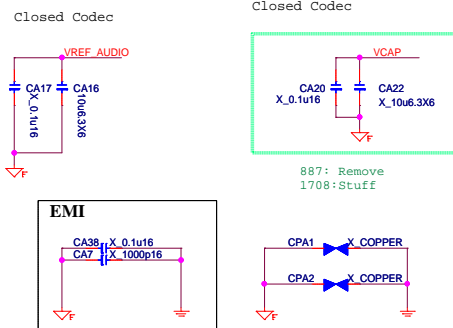
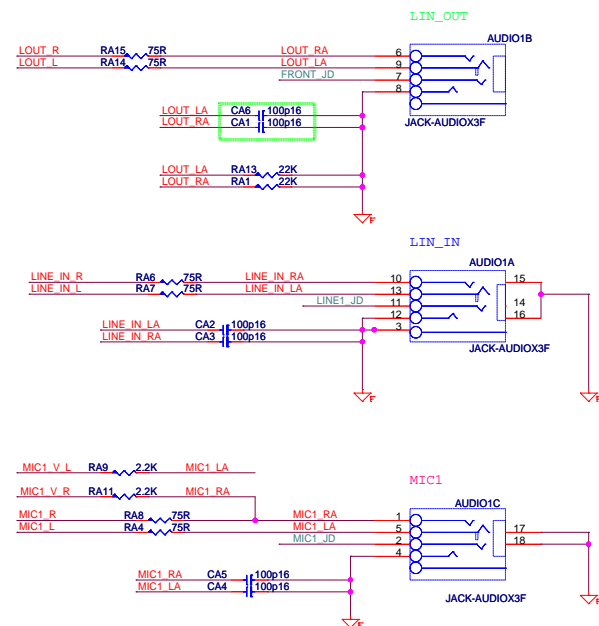
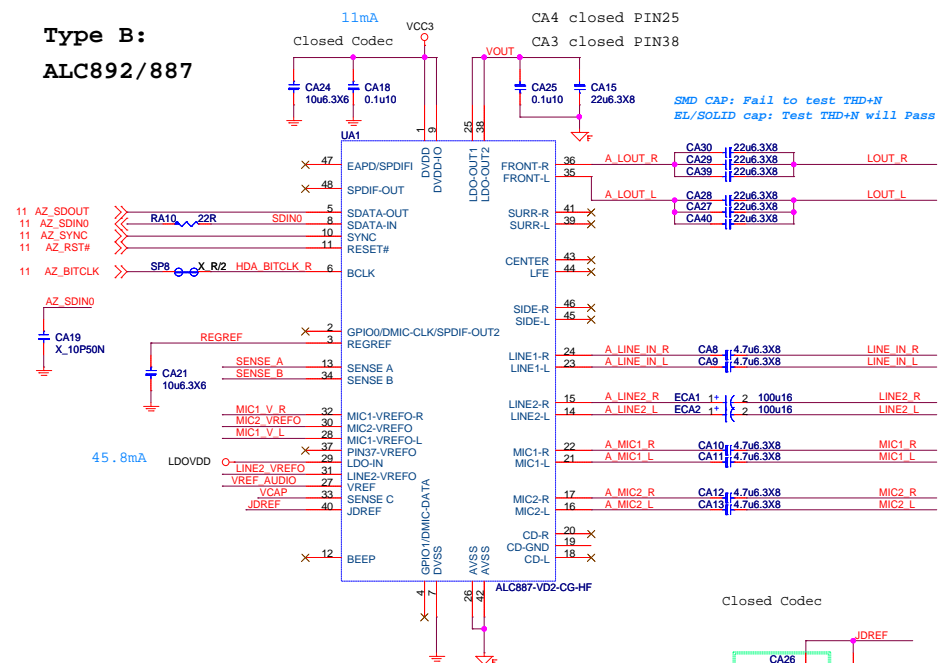
R466
X_180R/1%4

HDMI C. DATA2 N

HDMI C. DATA2 P

R469
X_180R/1%4

Type B:
ALC892/887



100pF Cap can change to
TVS by PM request.

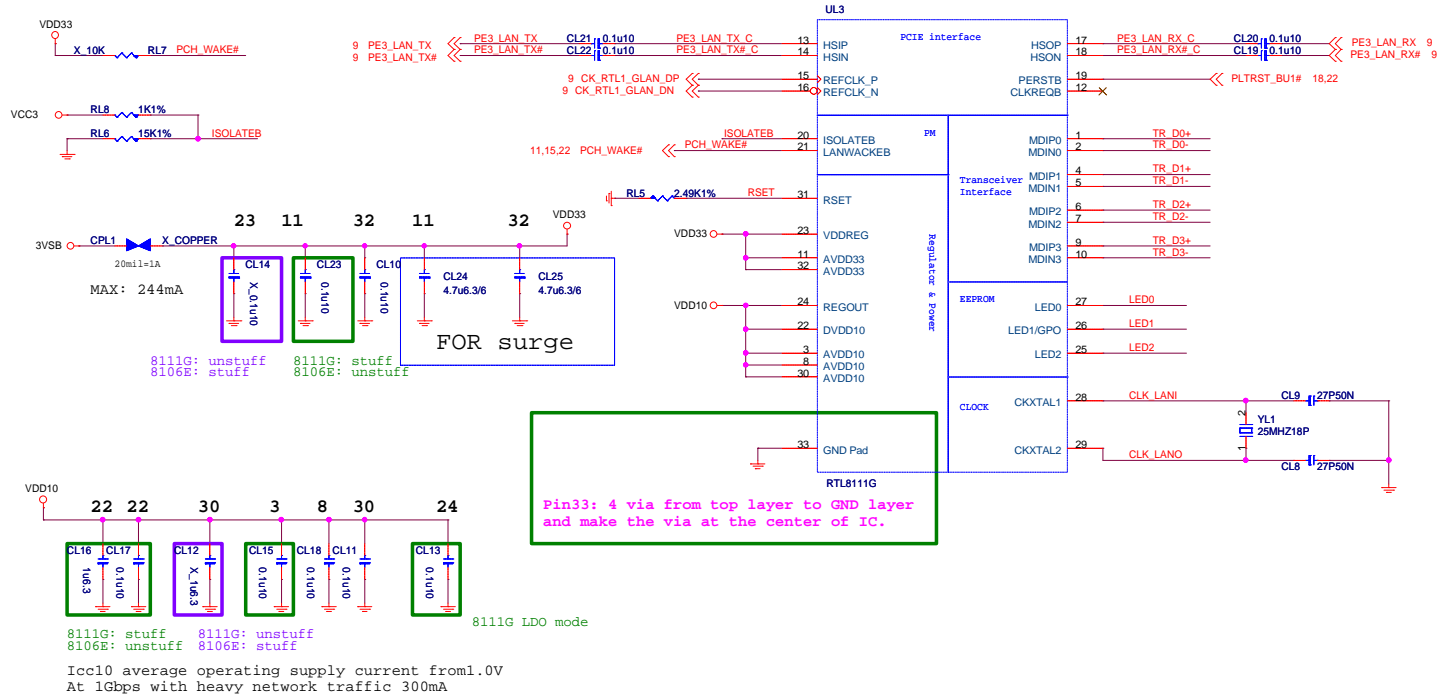


MICRO-STAR INT'L CO.,LTD			
MS-7846			
Size Custom	Document Description Audio Codec ALC892/887		Rev 2.1
Date: Monday, August 12, 2013		Sheet 19 of 38	

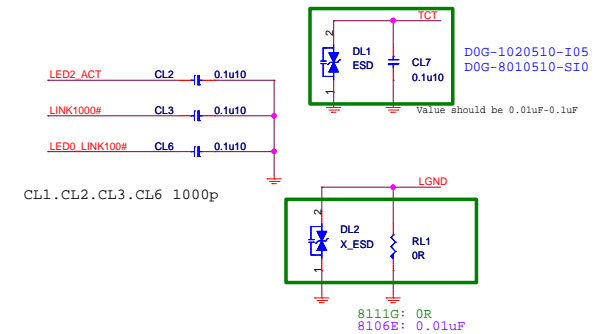
RTL8111G Giga LAN

RTL8106E 10/100M LAN

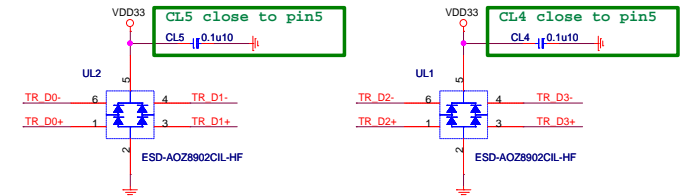
LAN Connector



8111G: Keep RL3 and Remove RL4 for RTL8111G
8106E: Keep RL4 and Remove RL3 for RTL8106E



Reserve ESD Protect



MSI P/N : D0G-0200529-A68, Vender P/N : AOZ8902CI
MSI P/N : D0G-0100619-I05, Vender P/N : TVLST2304AD0

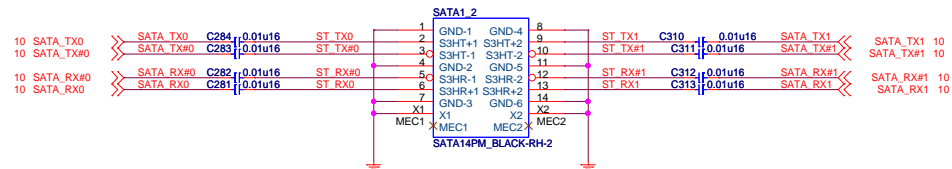
8106E POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	15/94	49.5/310.2
100 M Idle/TxRx	52/105	171.6/346.5
S0 ALDPS	4	13.2

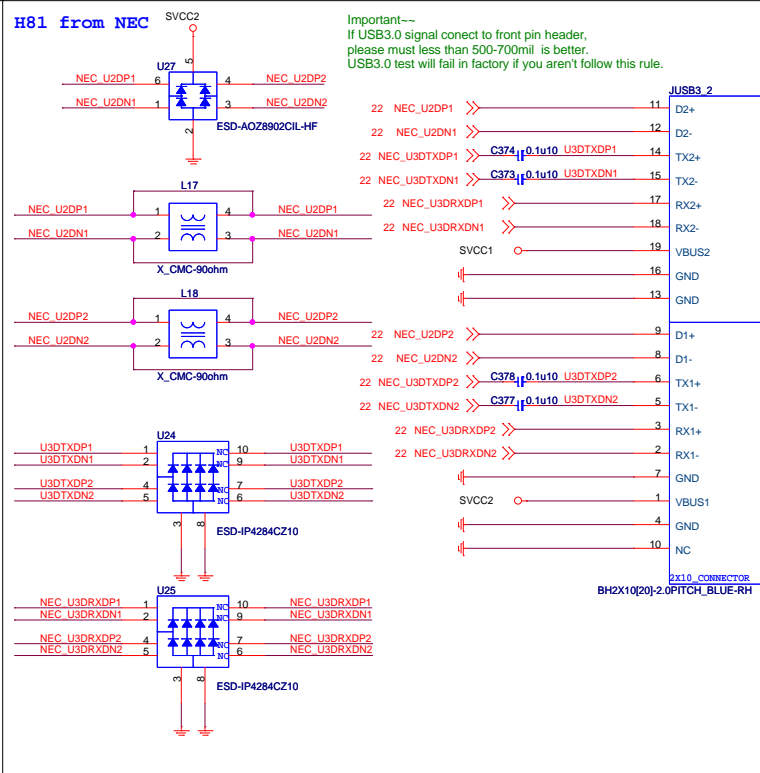
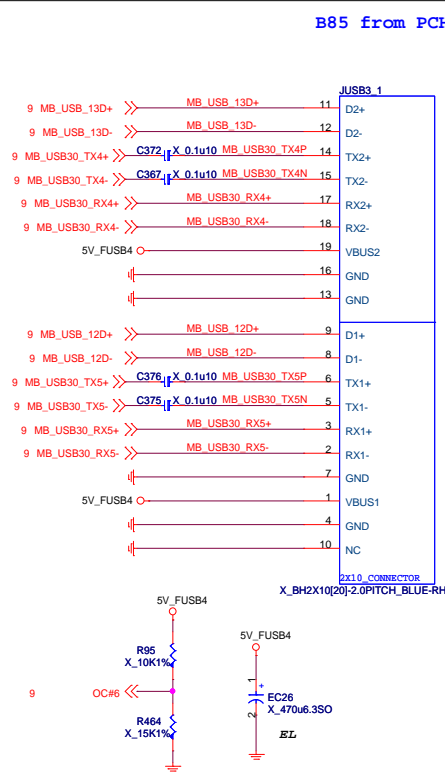
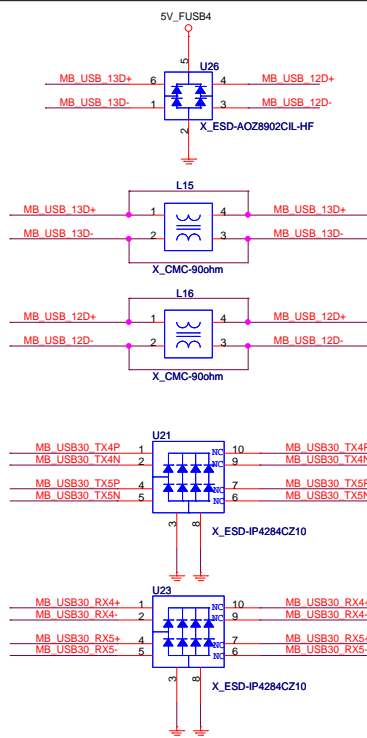
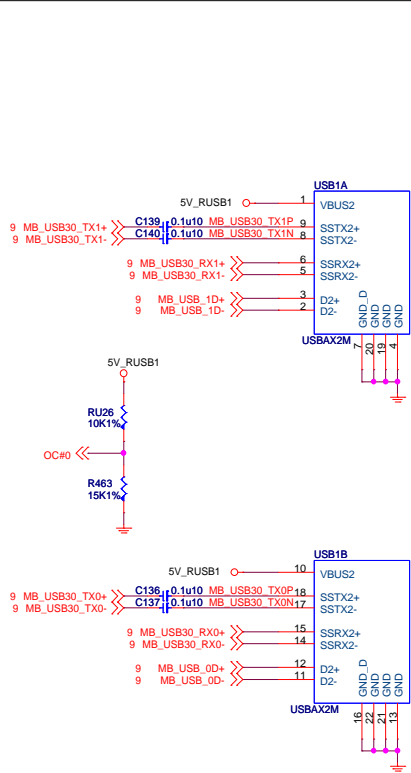
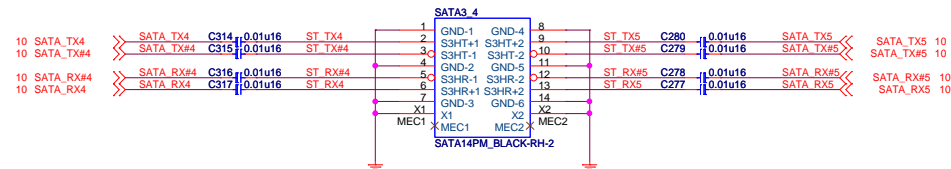
8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591.8/804.9
ALDPS	6.41	21.15

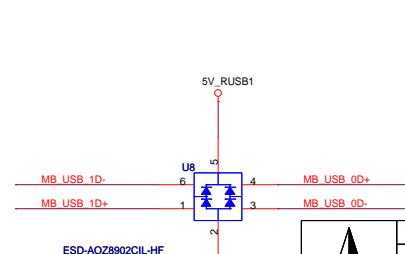
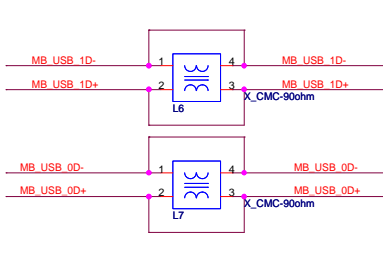
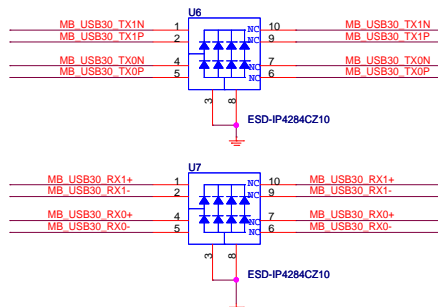
SATA 6G PORT 0,1



SATA 3G PORT 4,5



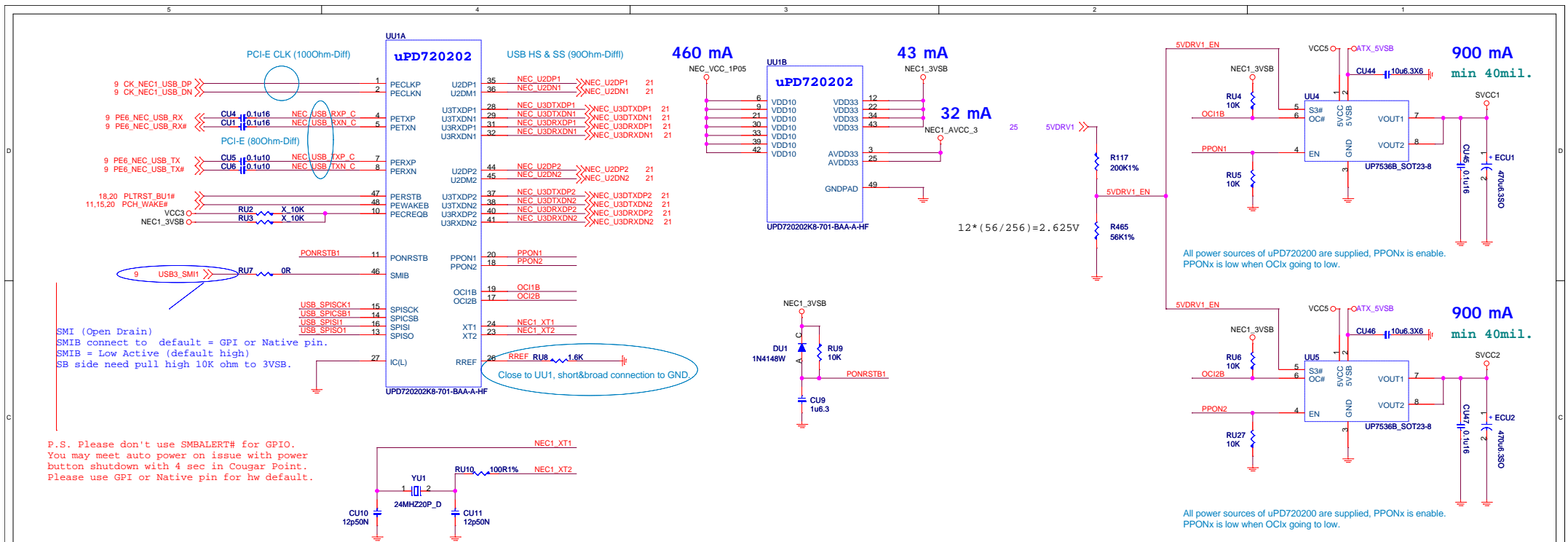
Important--
If USB3.0 signal connect to front pin header,
please must less than 500-700mil is better.
USB3.0 test will fail in factory if you aren't follow this rule.



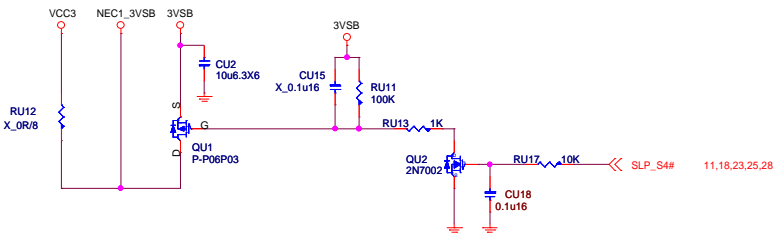
MICRO-STAR INT'L CO.,LTD

MS-7846

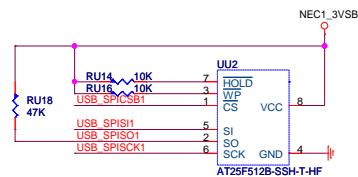
Size	Document Description	Rev
Custom	SATA Connector	2.1
Date: Monday, August 12, 2013	Sheet 21 of 38	



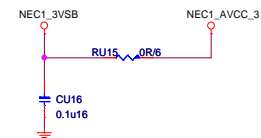
3V_Dual Circuit



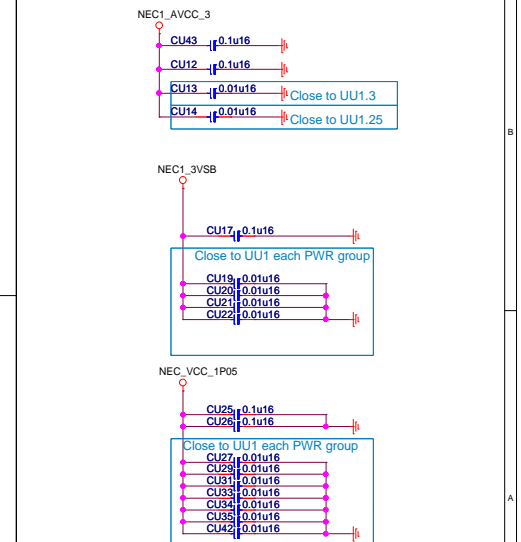
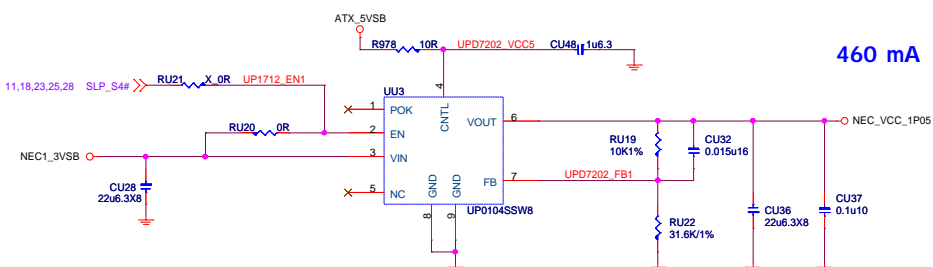
EEPROM



AVCC3 STB Power



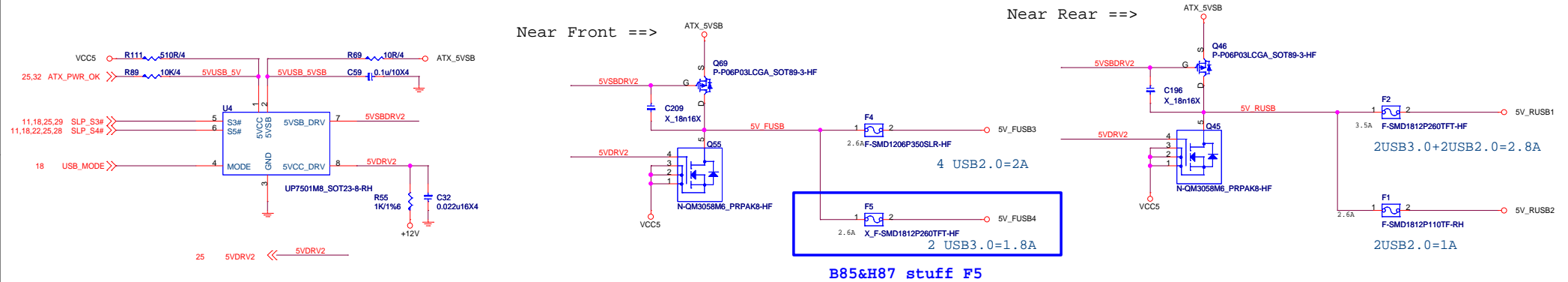
uPD720200 core Power



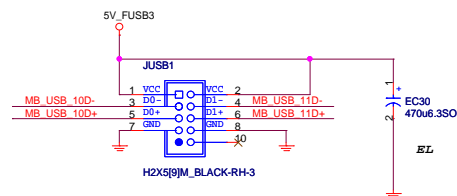
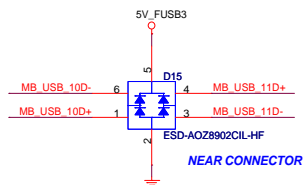
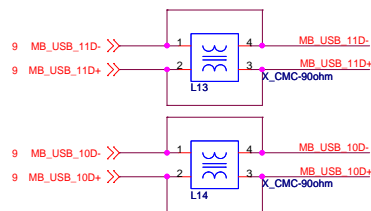
Type A: UP7501+MOS+Fuse

PCH/FCH side; OC# pull high to +3VSB

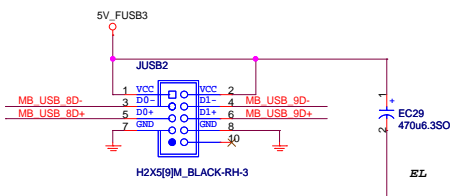
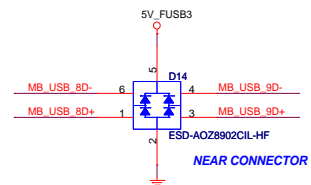
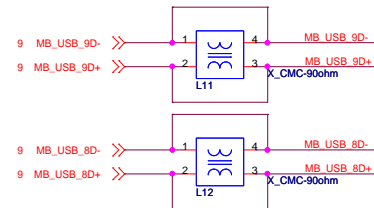
D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
 D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
 D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)
 D08-2000200-P16 (Itrip=3.5A; 0.003ohm) MINISMD050



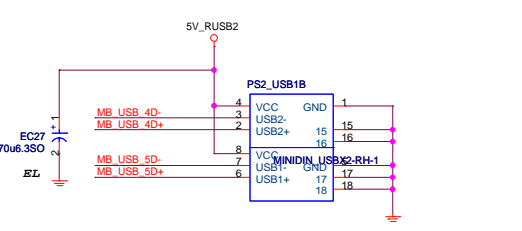
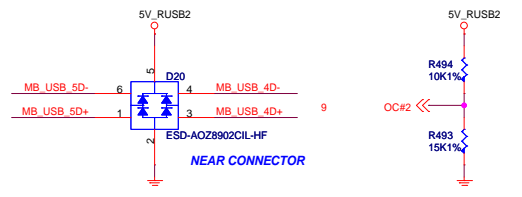
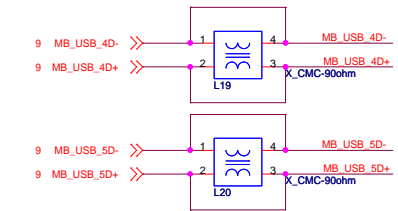
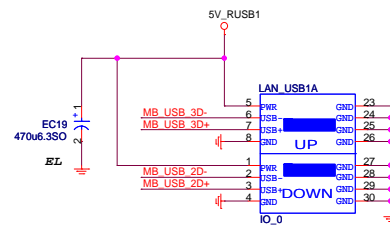
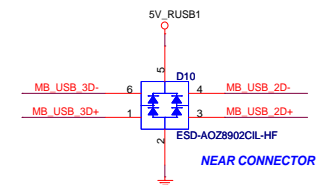
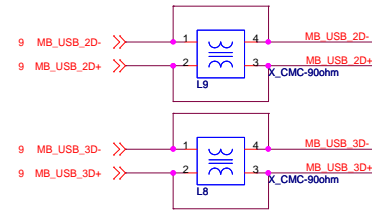
FRONT USB PORT 10,11



FRONT USB PORT 8,9

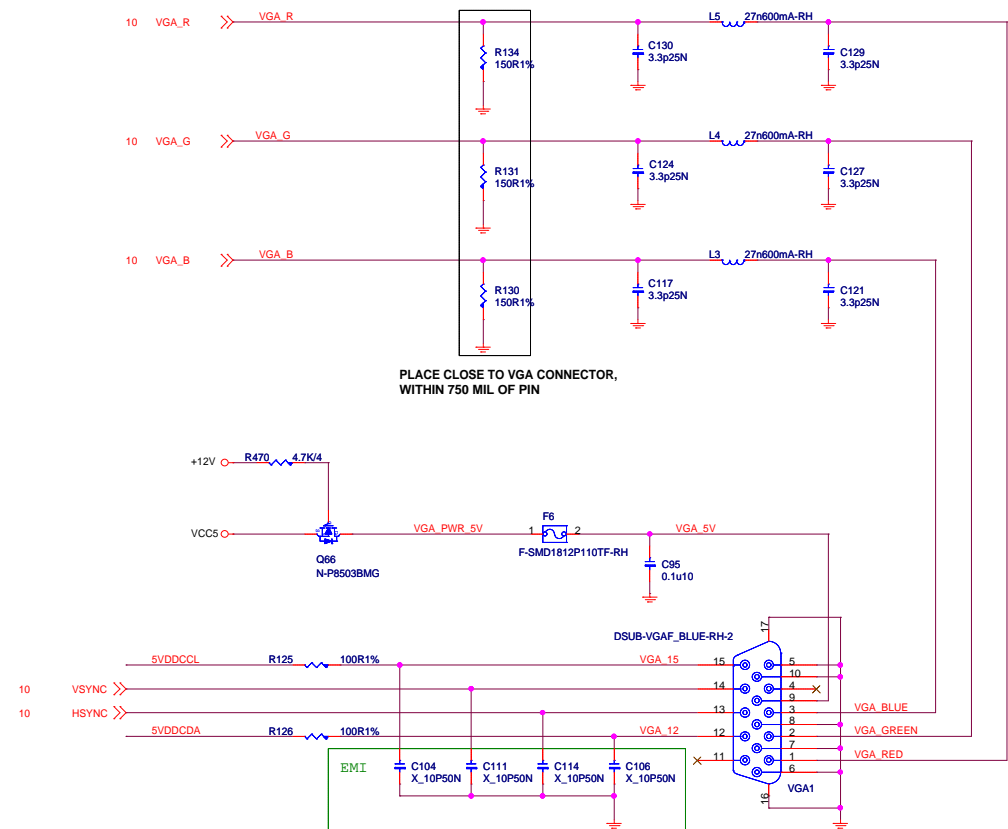
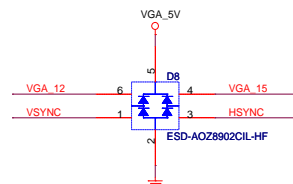
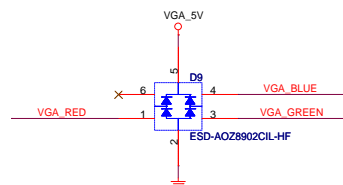
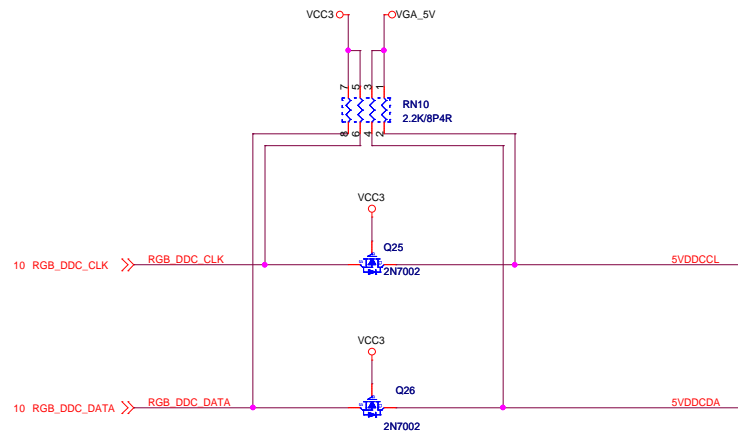


REAL USB PORT 12,13



D-Sub

Level shift



MICRO-STAR INT'L CO.,LTD

MS-7846

Size Custom	Document Description VGA Connector	Rev 2.1
Date: Monday, August 12, 2013		Sheet 24 of 38

5VDIMM FOR DDR

VCC5
23.32 ATX_PWR_OK
11.18,23.29 SLP_S3#
11.18,22.23,28 SLP_S4#
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

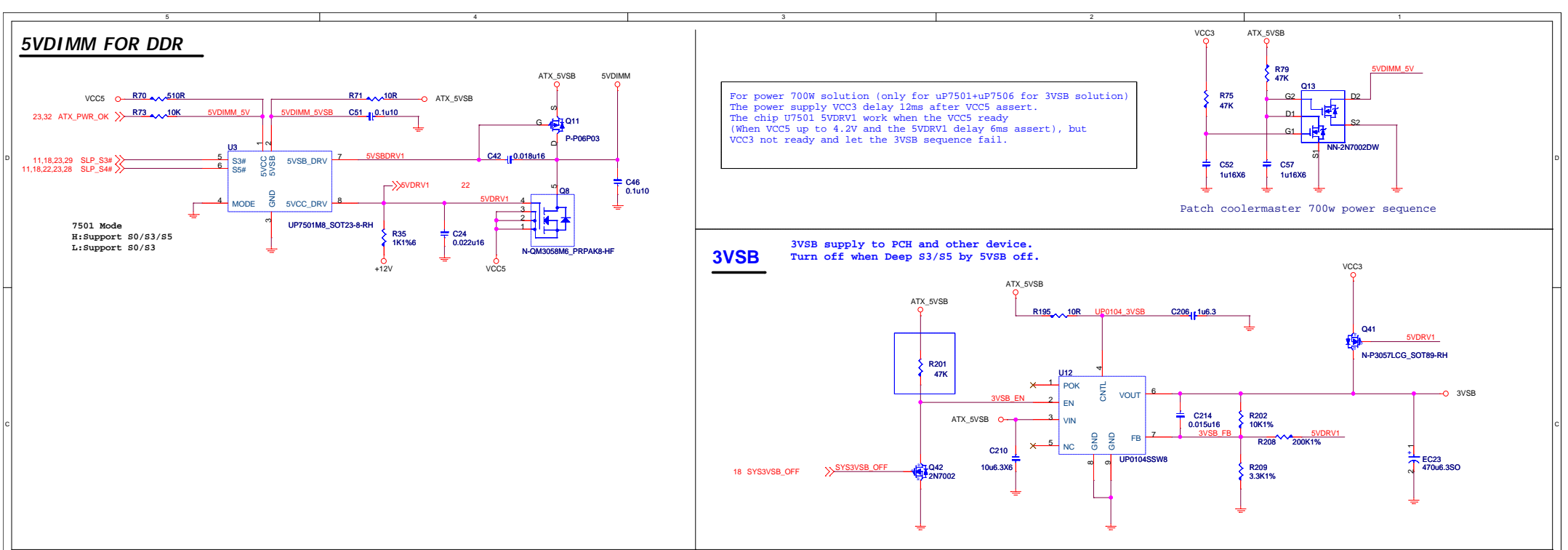
ATX_5VSB
5VDIMM
5VSDRV1
5VCC_DRV
5VSB
5VCC
MODE
GND
UP7501M8_SOT23-8-RH
N-QM3058M6_PRPAK8-HF
C42
C46
C51
C24
R70
R73
R71
R35
+12V
VCC5

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VSDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VSDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

Patch coolermaster 700w power sequence

3VSB

ATX_5VSB
3VSB_EN
3VSB_FB
3VSB
5VDRV1
VCC3
EC23
C210
C214
C206
R201
R195
R202
R208
R209
Q42
Q41
UP0104_3VSB
UP0104SSW8
N-P3057LCG_SOT89-RH
P-2N7002
18 SYS3VSB_OFF
SYS3VSB_OFF



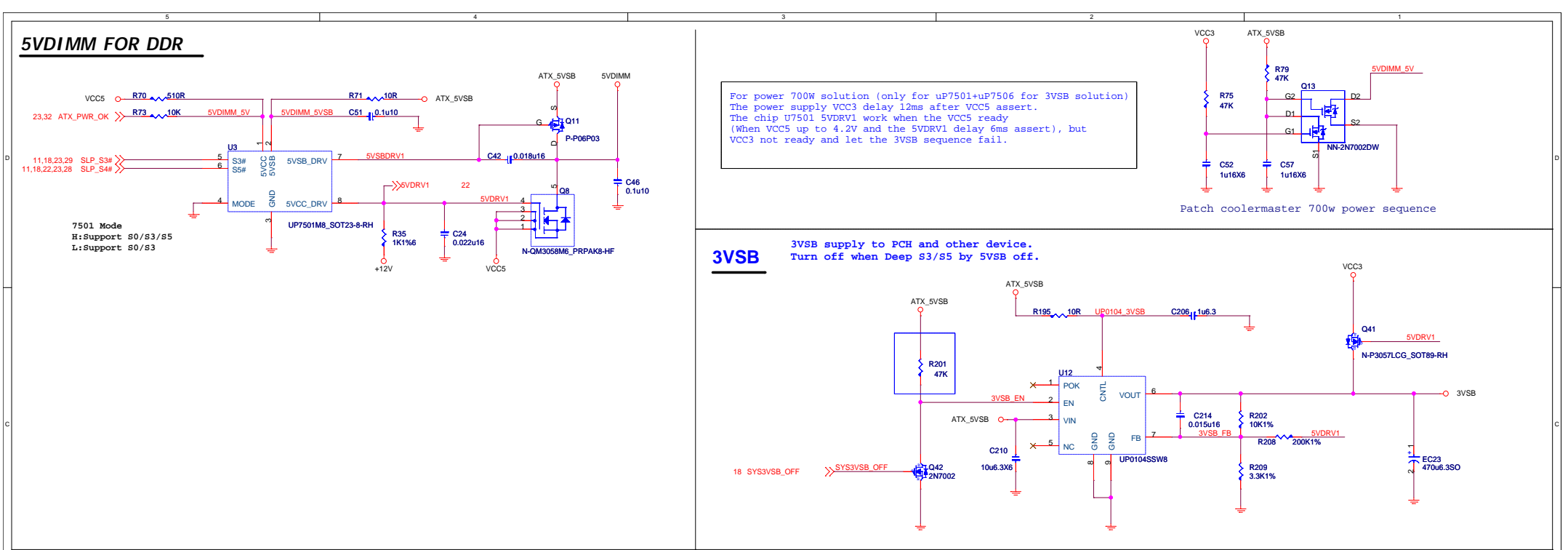
5VDIMM FOR DDR

7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

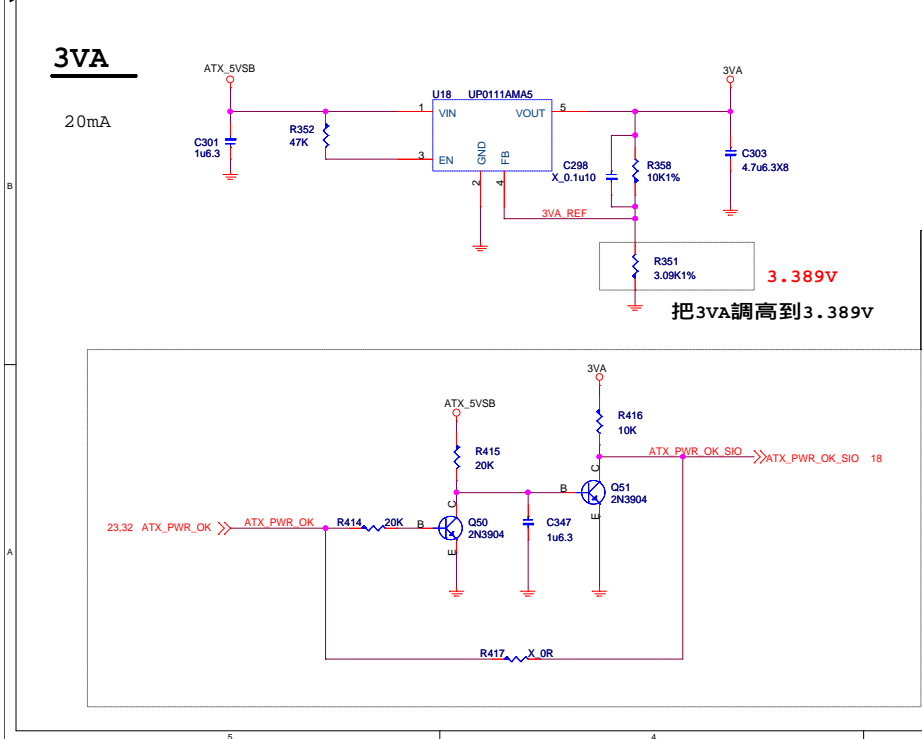
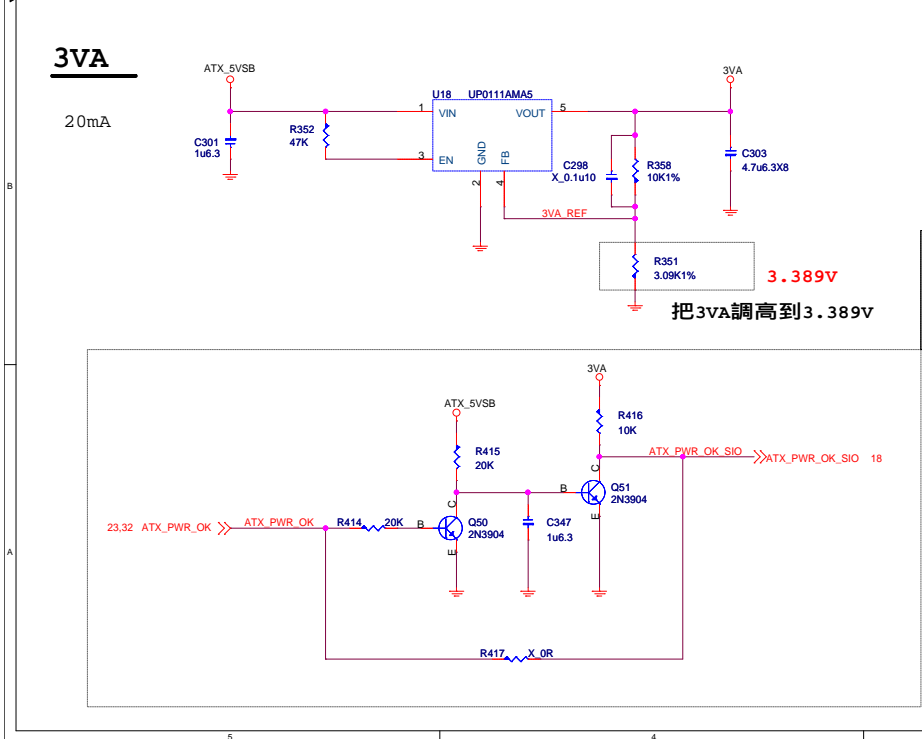
3VSB

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

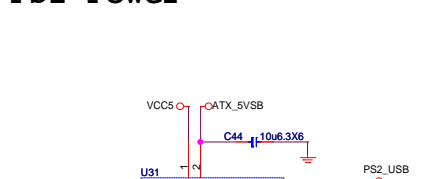
Patch coolermaster 700w power sequence



The diagram shows a 3V regulator circuit. The top part is a schematic of the regulator, featuring a U18 UP0111AMA5 IC. The input is ATX_5VSB, filtered by C301 (1u6.3). The output is 3V, filtered by C303 (4.7u6.3X8). The enable pin (EN) is connected to a 3V REF divider (R351, R358) and a 3V_A signal. The bottom part is a schematic of the enable logic, showing a 2N3904 transistor (Q51) that drives the EN pin. The base of Q51 is connected to ATX_PWR_OK_SIO through a 20K resistor (R414). The emitter is grounded, and the collector is connected to the EN pin. A 2N3904 transistor (Q50) is also shown, connected to the ATX_PWR_OK_SIO signal. The ATX_PWR_OK_SIO signal is also connected to the 3V_A signal through a 10K resistor (R416).




PS2 Power




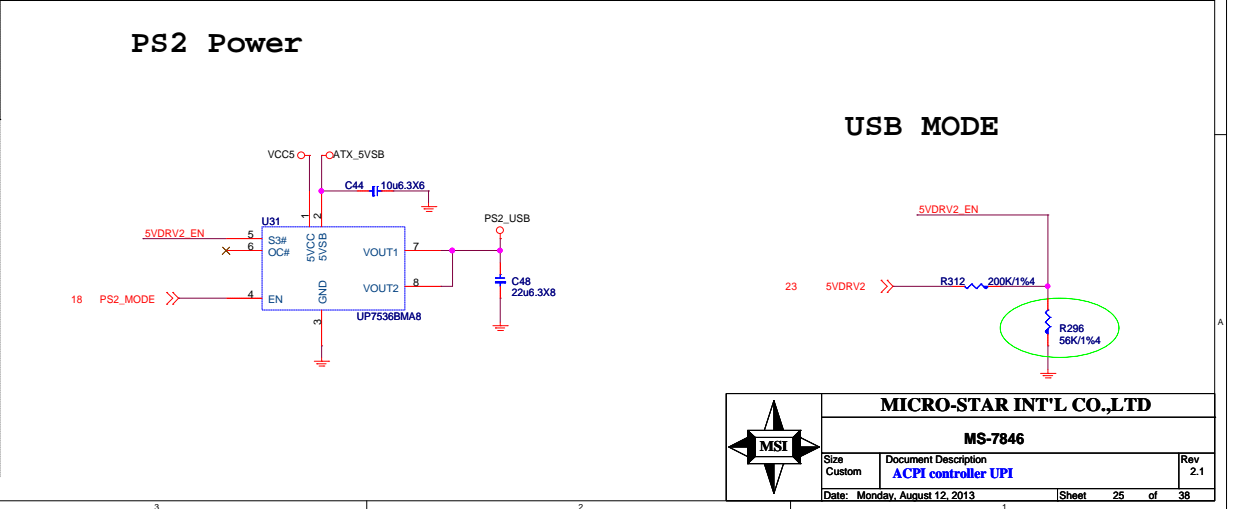
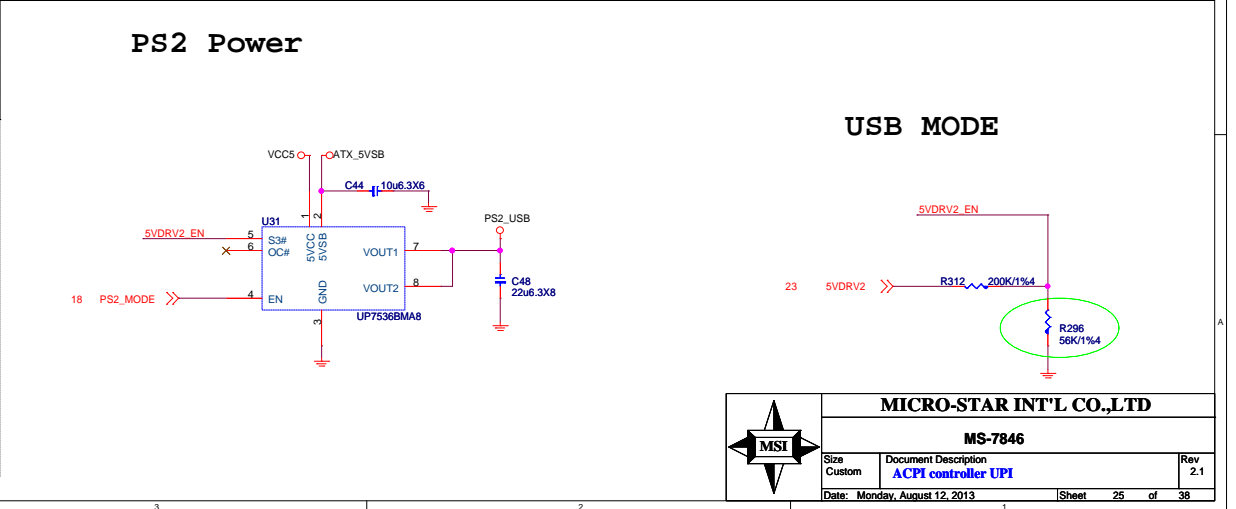
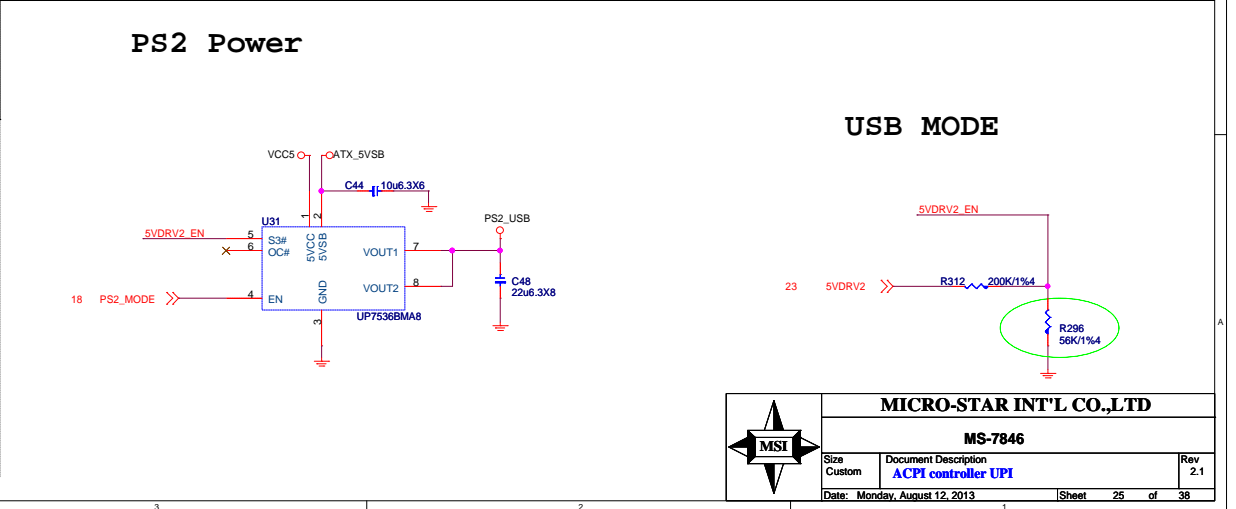
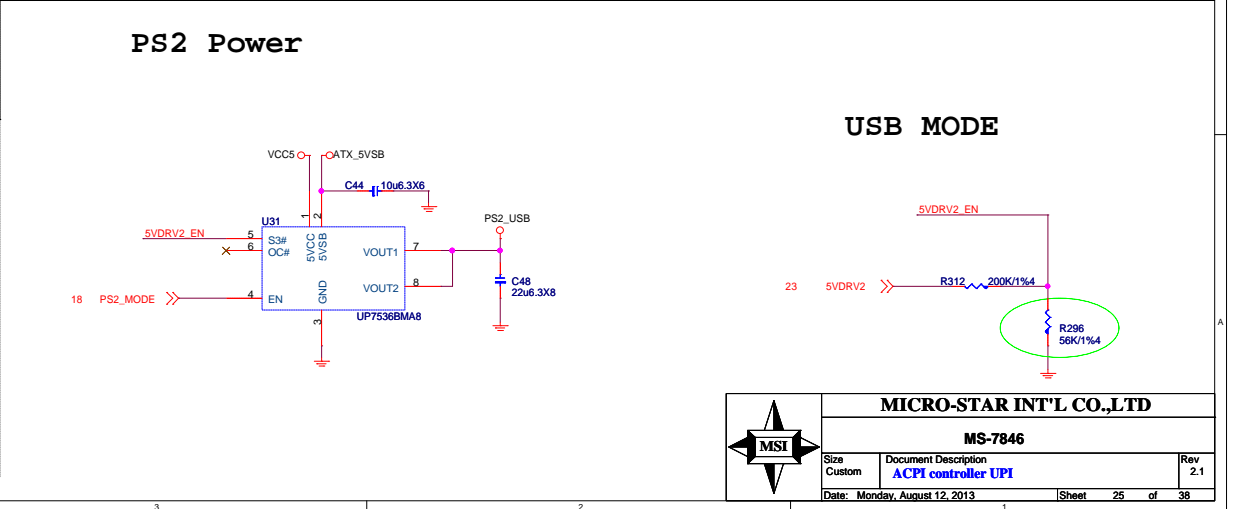
The PS2 Power circuit diagram shows a voltage regulator U31 (UP7536BMA8) converting ATX_5VSB to PS2_USB. The regulator's input (VIN) is connected to ATX_5VSB through a 10µF 3X6 capacitor C44. The output (VOUT1) is connected to PS2_USB through a 22µF 3X6 capacitor C48. The regulator's EN pin is connected to PS2_MODE, and its GND pin is connected to GND. The regulator's VIN pin is also connected to 5VDRV2_EN. The regulator's VOUT2 pin is connected to GND.

USB MODE

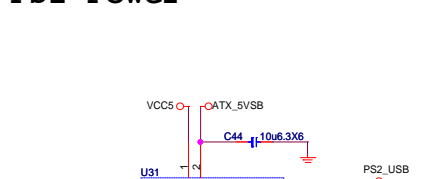


The USB MODE circuit diagram shows a pull-up resistor R296 (56K 1% 4) connected to 5VDRV2_EN and a pull-down resistor R312 (200K 1% 4) connected to PS2_USB. The circuit is labeled with 23 5VDRV2 and 23 PS2_USB.

		MICRO-STAR INT'L CO.,LTD	
		MS-7846	
Size Custom	Document Description ACPI controller UPI		Rev 2.1
Date: Monday, August 12, 2013		Sheet	25 of 38




PS2 Power




The PS2 Power circuit diagram shows a voltage regulator U31 (UP7536BMA8) converting ATX_5VSB to PS2_USB. The regulator's input (VIN) is connected to ATX_5VSB through a 10µF 3X6 capacitor C44. The output (VOUT1) is connected to PS2_USB through a 22µF 3X6 capacitor C48. The regulator's EN pin is connected to PS2_MODE, and its GND pin is connected to GND. The regulator's VIN pin is also connected to 5VDRV2_EN. The regulator's VOUT2 pin is connected to GND.

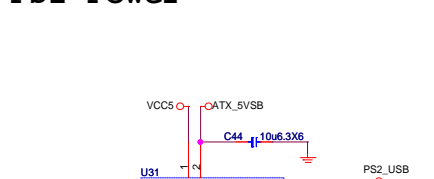
USB MODE



The USB MODE circuit diagram shows a pull-up resistor R296 (56K 1% 4) connected to 5VDRV2_EN and a pull-down resistor R312 (200K 1% 4) connected to PS2_USB. The circuit is labeled with 23 5VDRV2 and 23 PS2_USB.


		MICRO-STAR INT'L CO.,LTD	
		MS-7846	
Size Custom	Document Description ACPI controller UPI		Rev 2.1
Date: Monday, August 12, 2013		Sheet	25 of 38

PS2 Power




The PS2 Power circuit diagram shows a voltage regulator U31 (UP7536BMA8) converting ATX_5VSB to PS2_USB. The regulator's input (VIN) is connected to ATX_5VSB through a 10µF 3X6 capacitor C44. The output (VOUT1) is connected to PS2_USB through a 22µF 3X6 capacitor C48. The regulator's EN pin is connected to PS2_MODE, and its GND pin is connected to GND. The regulator's VIN pin is also connected to 5VDRV2_EN. The regulator's VOUT2 pin is connected to GND.

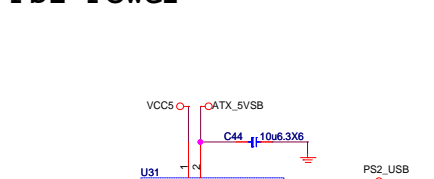
USB MODE



The USB MODE circuit diagram shows a pull-up resistor R296 (56K 1% 4) connected to 5VDRV2_EN and a pull-down resistor R312 (200K 1% 4) connected to PS2_USB. The circuit is labeled with 23 5VDRV2 and 23 PS2_USB.


		MICRO-STAR INT'L CO.,LTD	
		MS-7846	
Size Custom	Document Description ACPI controller UPI		Rev 2.1
Date: Monday, August 12, 2013		Sheet	25 of 38

PS2 Power




The PS2 Power circuit diagram shows a voltage regulator U31 (UP7536BMA8) converting ATX_5VSB to PS2_USB. The regulator's input (VIN) is connected to ATX_5VSB through a 10µF 3X6 capacitor C44. The output (VOUT1) is connected to PS2_USB through a 22µF 3X6 capacitor C48. The regulator's EN pin is connected to PS2_MODE, and its GND pin is connected to GND. The regulator's VIN pin is also connected to 5VDRV2_EN. The regulator's VOUT2 pin is connected to GND.

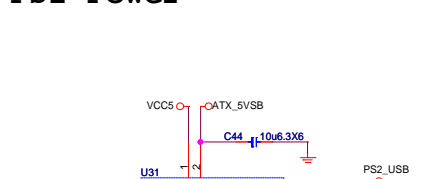
USB MODE



The USB MODE circuit diagram shows a pull-up resistor R296 (56K 1% 4) connected to 5VDRV2_EN and a pull-down resistor R312 (200K 1% 4) connected to PS2_USB. The circuit is labeled with 23 5VDRV2 and 23 PS2_USB.


		MICRO-STAR INT'L CO.,LTD	
		MS-7846	
Size Custom	Document Description ACPI controller UPI		Rev 2.1
Date: Monday, August 12, 2013		Sheet	25 of 38

PS2 Power




The PS2 Power circuit diagram shows a voltage regulator U31 (UP7536BMA8) converting ATX_5VSB to PS2_USB. The regulator's input (VIN) is connected to ATX_5VSB through a 10µF 3X6 capacitor C44. The output (VOUT1) is connected to PS2_USB through a 22µF 3X6 capacitor C48. The regulator's EN pin is connected to PS2_MODE, and its GND pin is connected to GND. The regulator's VIN pin is also connected to 5VDRV2_EN. The regulator's VOUT2 pin is connected to GND.

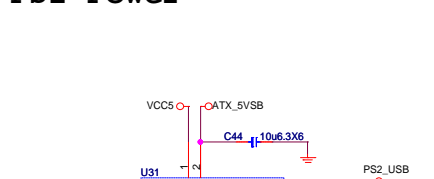
USB MODE



The USB MODE circuit diagram shows a pull-up resistor R296 (56K 1% 4) connected to 5VDRV2_EN and a pull-down resistor R312 (200K 1% 4) connected to PS2_USB. The circuit is labeled with 23 5VDRV2 and 23 PS2_USB.


		MICRO-STAR INT'L CO.,LTD	
		MS-7846	
Size Custom	Document Description ACPI controller UPI		Rev 2.1
Date: Monday, August 12, 2013		Sheet	25 of 38

PS2 Power




The PS2 Power circuit diagram shows a voltage regulator U31 (UP7536BMA8) converting ATX_5VSB to PS2_USB. The regulator's input (VIN) is connected to ATX_5VSB through a 10µF 3X6 capacitor C44. The output (VOUT1) is connected to PS2_USB through a 22µF 3X6 capacitor C48. The regulator's EN pin is connected to PS2_MODE, and its GND pin is connected to GND. The regulator's VIN pin is also connected to 5VDRV2_EN. The regulator's VOUT2 pin is connected to GND.

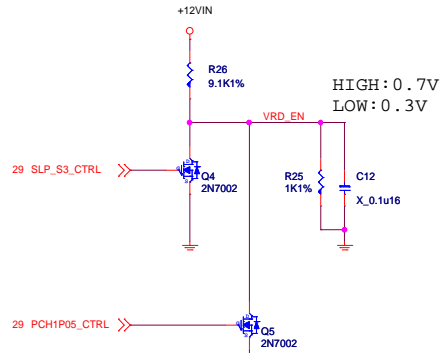
USB MODE



The USB MODE circuit diagram shows a pull-up resistor R296 (56K 1% 4) connected to 5VDRV2_EN and a pull-down resistor R312 (200K 1% 4) connected to PS2_USB. The circuit is labeled with 23 5VDRV2 and 23 PS2_USB.

		MICRO-STAR INT'L CO.,LTD	
		MS-7846	
Size Custom	Document Description ACPI controller UPI		Rev 2.1
Date: Monday, August 12, 2013		Sheet	25 of 38

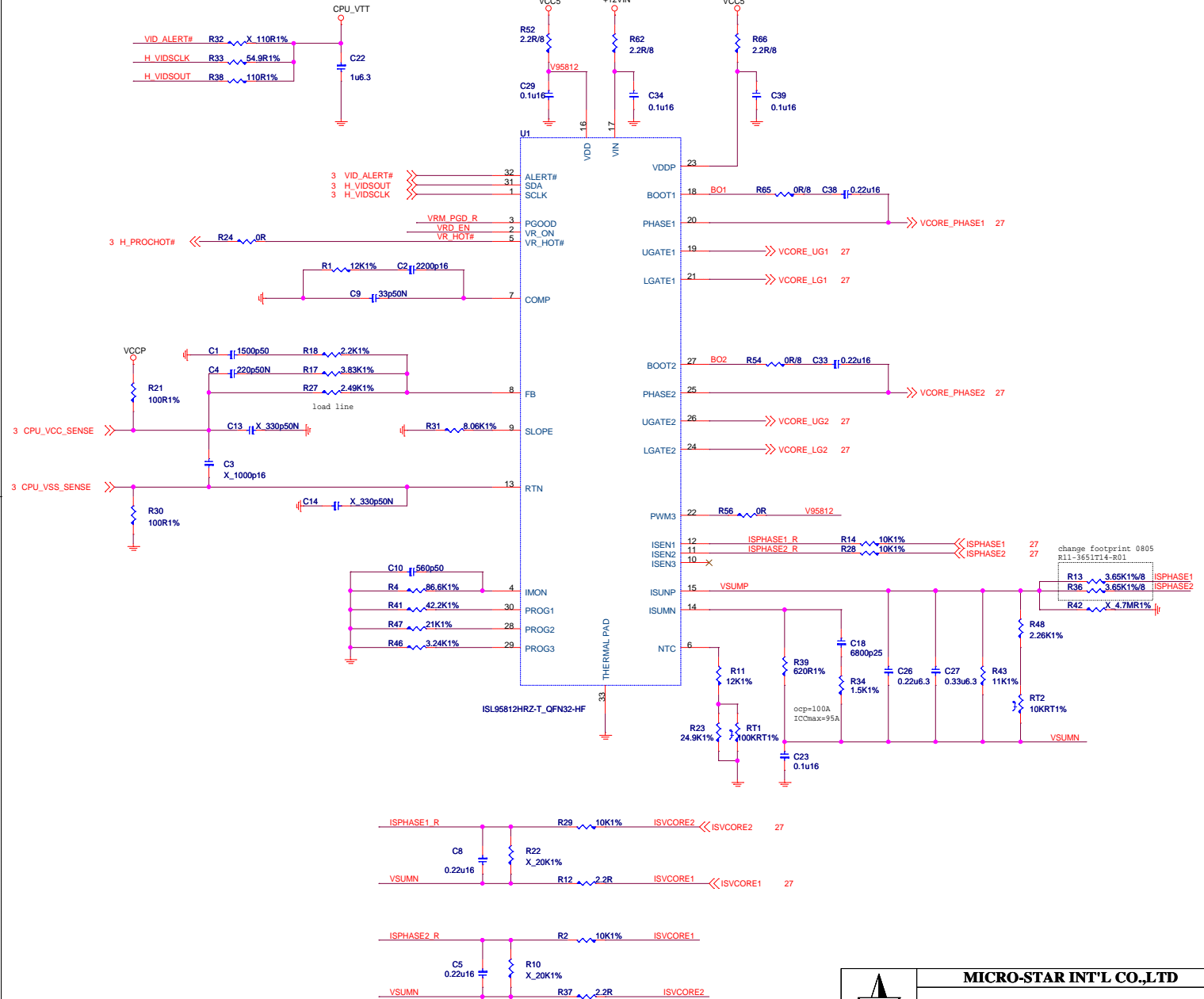
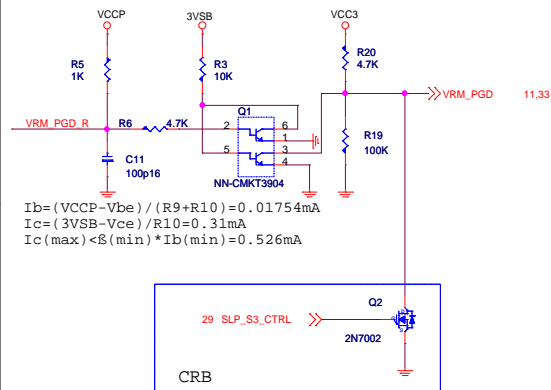
VCORE power on by s3 and 12v



CRB

HIGH:by PCH_1P05V
LOW:by S3

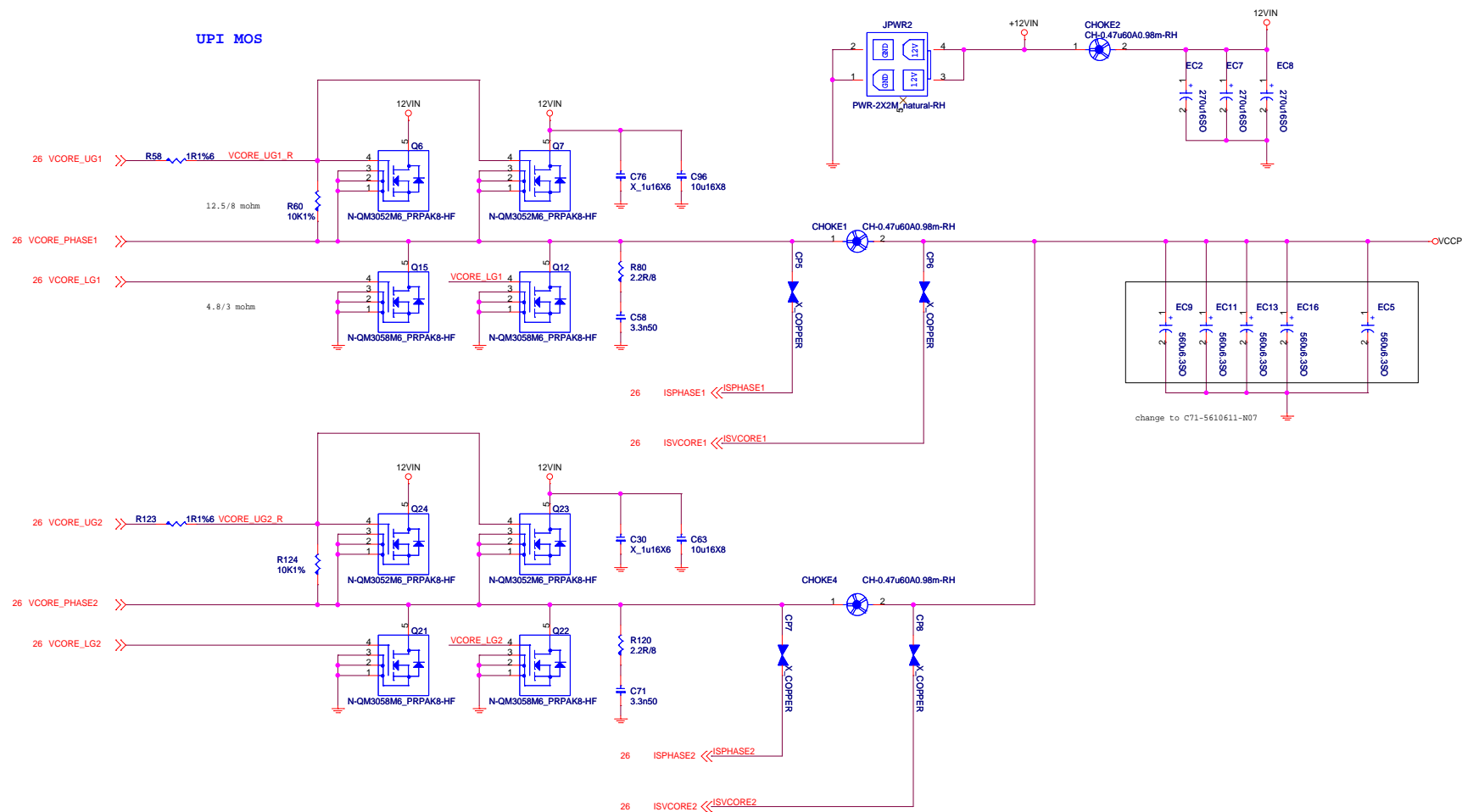
VRMPWRGD LEVEL SHIFT



VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm

Irms_input=17.5A



DDR Power:1.5V

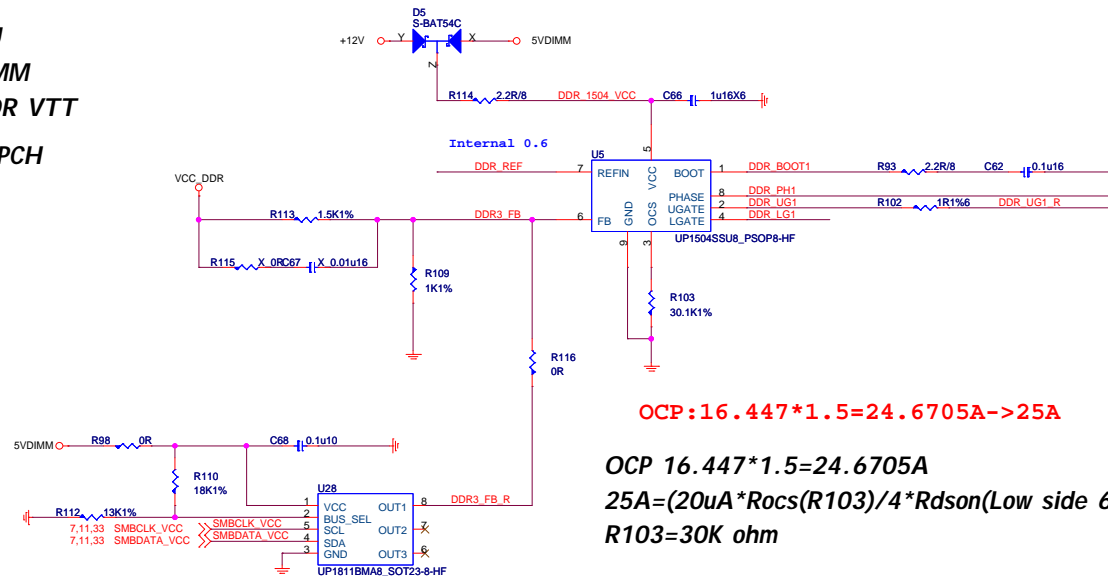
DDR3_1.5V 4.2A+6A+0.5A+5.747=16.447A

4.2A FOR CPU

6A FOR 2DIMM

0.5A FOR DDR VTT

5.747A FOR PCH

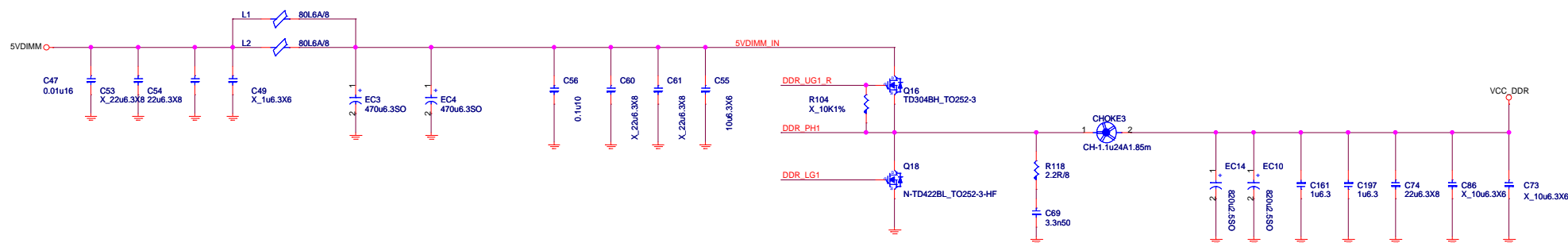


OCP:16.447*1.5=24.6705A->25A

OCP 16.447*1.5=24.6705A

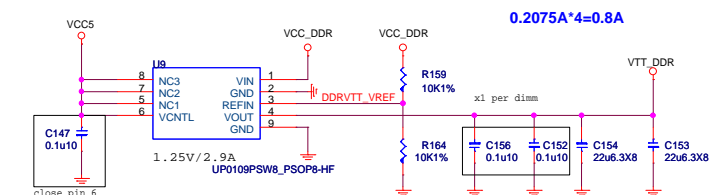
25A=(20uA*Rocs(R103)/4*Rdson(Low side 6mohm)

R103=30K ohm



DDR VTT Power

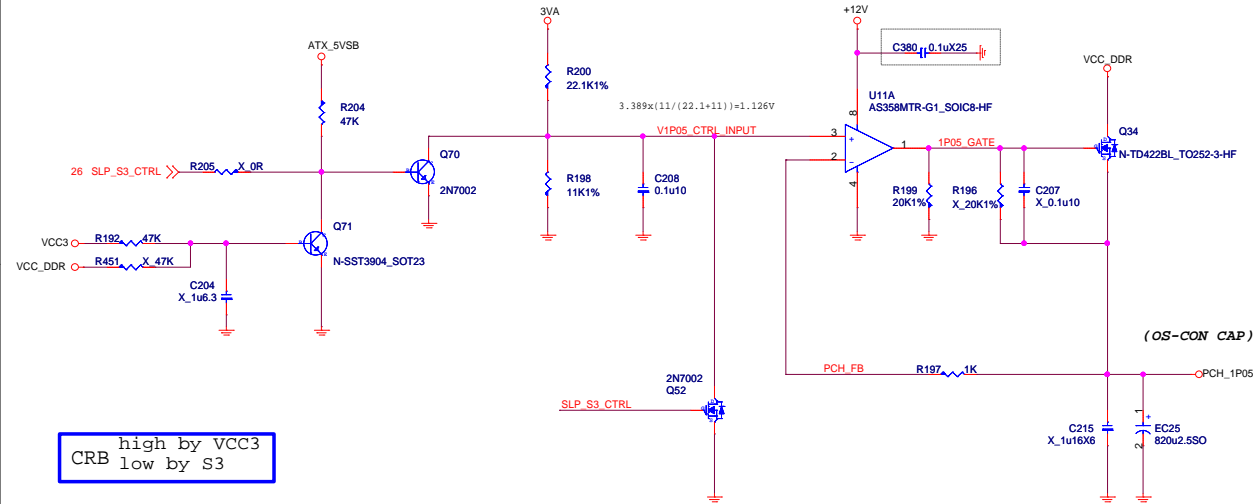
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



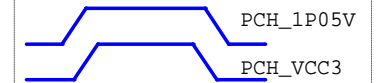
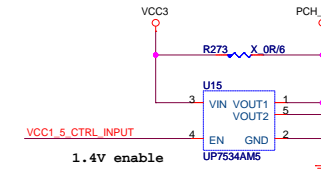
P.S. Only for meet Intel power down sequence.

MICRO-STAR INT'L CO.,LTD			
MS-7846			
Size	Document Description	Rev	
Custom	DDR Power -UP6103 1-Phase	2.1	
Date:	Monday, August 12, 2013	Sheet	28 of 38

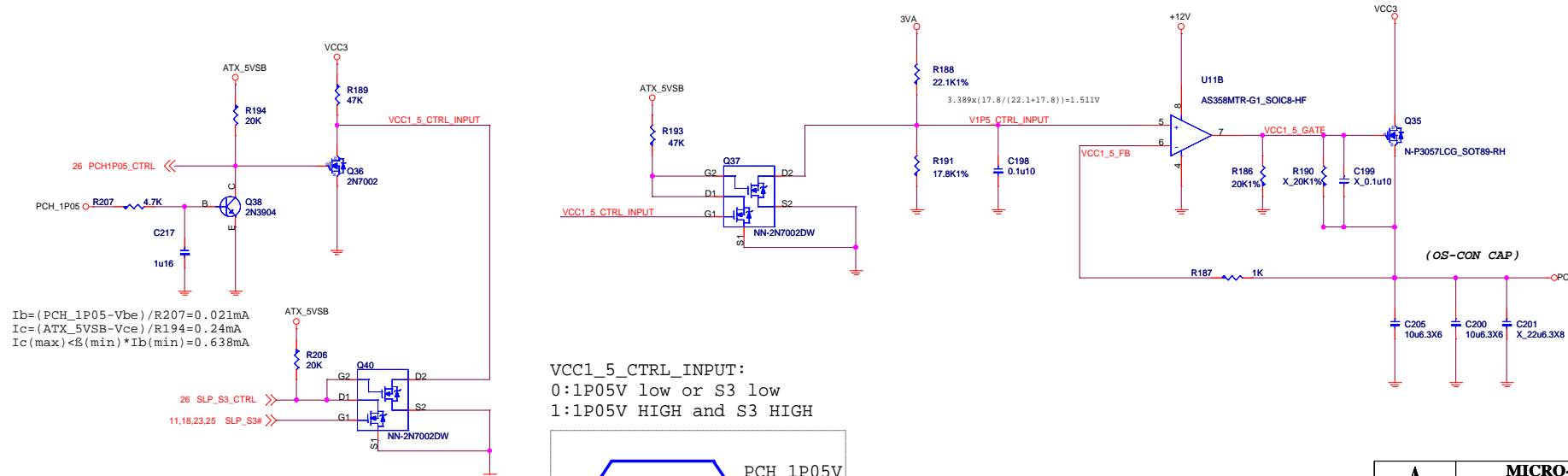
PCH Power:1.05V 5.747A



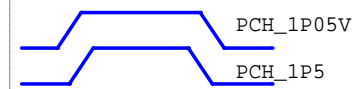
0.133A



PCH Power:1.5V 0.183A



VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

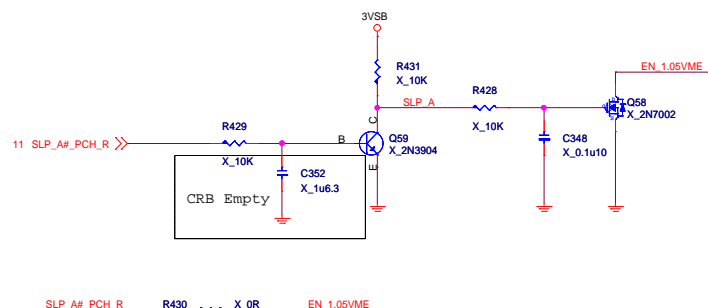


	MICRO-STAR INT'L CO.,LTD		
	MS-7846		
	Size Custom	Document Description PCH Power - OP+MOS	Rev 2.1
	Date: Monday, August 12, 2013	Sheet 29 of 38	

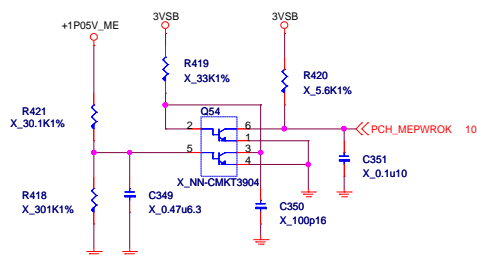
PCH ME Power:1.05V 0.670A

SLP_A

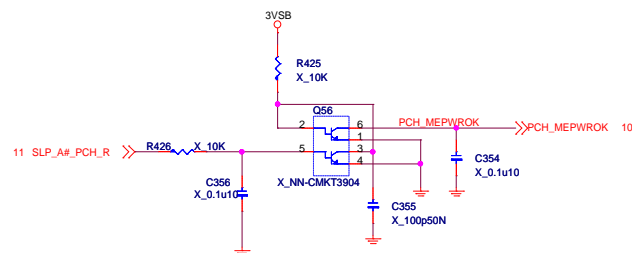
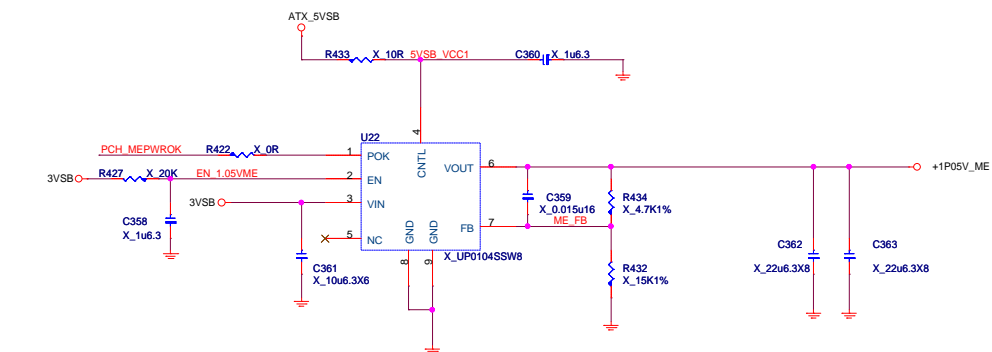
ME Power Control



PCH MEPWROK

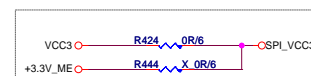


VccASW active to APWROK high 1ms



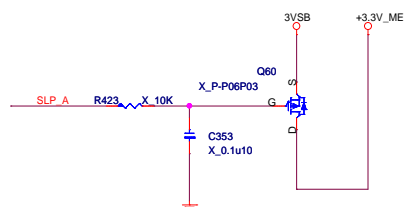
APWROK falling to VccASW falling 40ns

FOR INTEL ME



H81 stuff R424
B85 stuff R444

+3.3V_ME

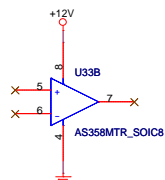
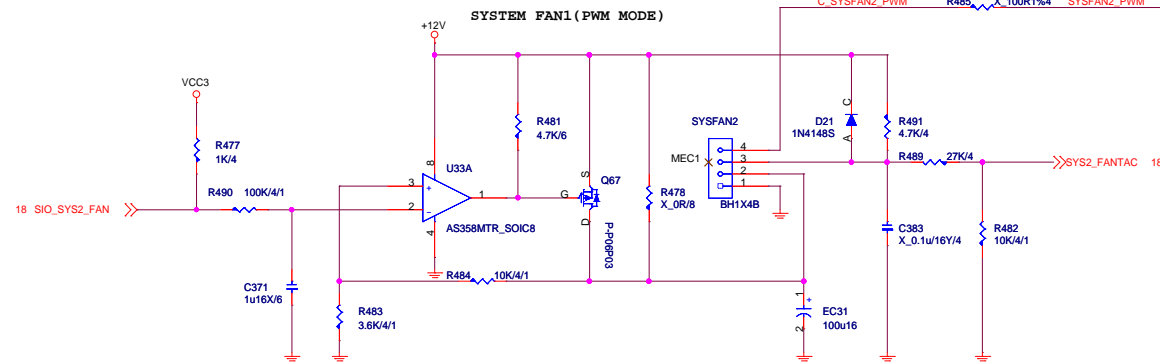
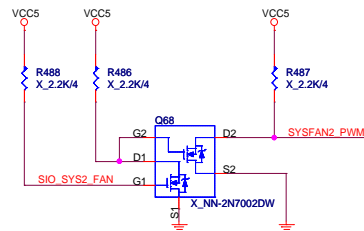
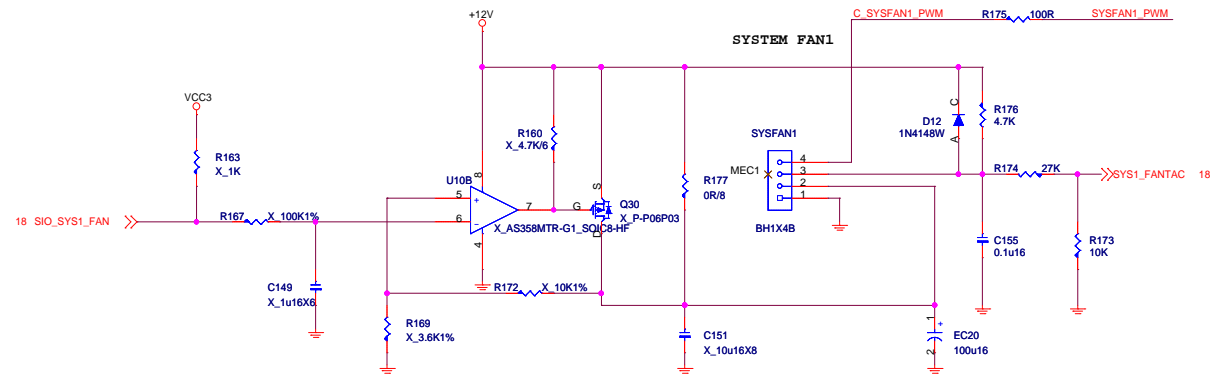
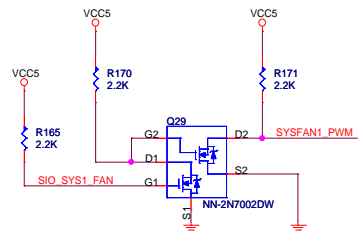
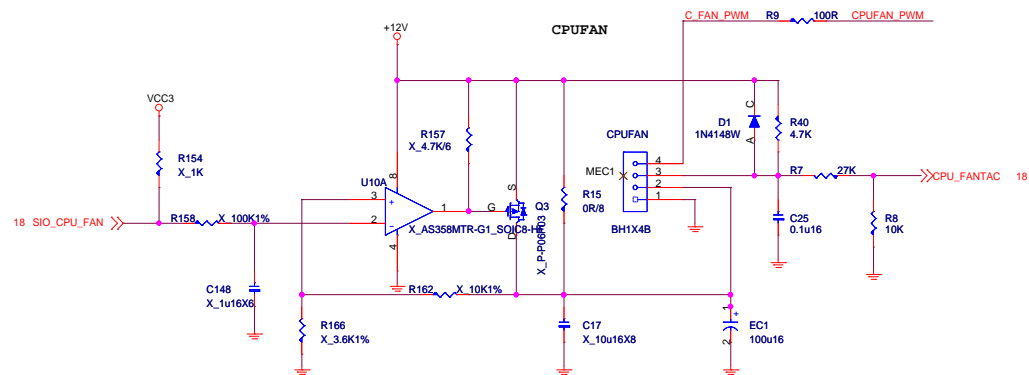
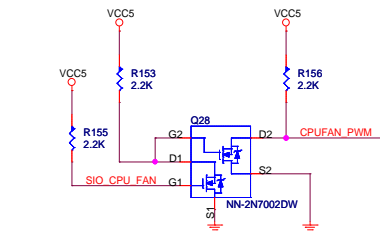


FAN-COUNTROL CIRCUIT

FAN TYPE E

FAN TYPE E

FAN TYPE F



The schematic diagram illustrates the power supply section of a circuit board. It features a JPWR1 connector with pins 1 through 24. The connections are as follows:

- Pin 1:** 3.3V, connected to VCC3.
- Pin 2:** 3.3V, connected to VCC3.
- Pin 3:** -12V, connected to -12V.
- Pin 4:** 3.3V, connected to VCC3.
- Pin 5:** GND, connected to GND.
- Pin 6:** GND, connected to GND.
- Pin 7:** 5V, connected to VCC5.
- Pin 8:** GND, connected to GND.
- Pin 9:** -5V, connected to POK.
- Pin 10:** 5V, connected to VCC5.
- Pin 11:** 5VSB, connected to +12V.
- Pin 12:** +12V, connected to +12V.
- Pin 13:** 5V, connected to VCC5.
- Pin 14:** GND, connected to GND.
- Pin 15:** GND, connected to GND.
- Pin 16:** P_ON, connected to PS_ON#.
- Pin 17:** GND, connected to GND.
- Pin 18:** GND, connected to GND.
- Pin 19:** GND, connected to GND.
- Pin 20:** GND, connected to GND.
- Pin 21:** -5V, connected to POK.
- Pin 22:** 5V, connected to VCC5.
- Pin 23:** 5VSB, connected to +12V.
- Pin 24:** +12V, connected to +12V.

Additional components and connections include:

- Resistors:** R161 (10K) between ATX_5VSB and VCC3; R168 (100R1%) between PS_ON# and VCC3; R144 (4.7K) between VCC5 and ATX_PWR_OK; R143 (1K) between VCC5 and ATX_5VSB.
- Capacitors:** C159 (X 0.1u10) between VCC3 and GND; C160 (0.1u16) between -12V and GND; C157 (X 0.1u10) between VCC3 and GND; C145 (X 0.1u10) between VCC5 and GND; C144 (X 0.1u10) between VCC5 and GND; C142 (0.1u16) between +12V and GND; C135 (X 0.1u16) between VCC3 and GND; C100 (X 0.1u10) between VCC5 and GND.
- Diode:** D11 (X_ESD-SFD0402) connected between PS_ON# and GND.
- Other:** ATX_5VSB is connected to GND; EC24 (470u6.3S0) is connected between GND and a power plane.

[illegible]

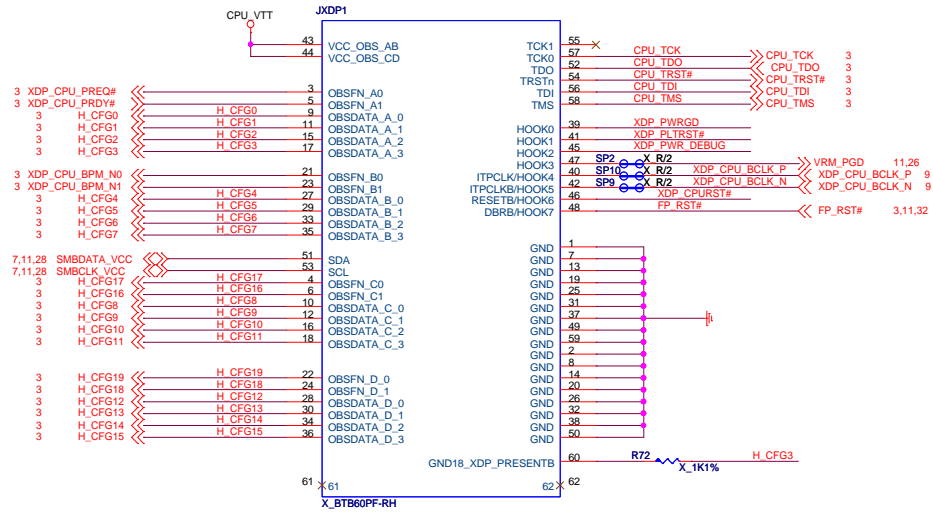
Pin connection diagram for the H2X710M-2PITCH_BLACK-RH module. The diagram shows a 14-pin connector with pins 1 through 14. Pin 1 is TPM_CLK, Pin 2 is 3VSB, Pin 3 is PE_S_RESET_N, Pin 4 is LPC_ADO, Pin 5 is LPC_ADO1, Pin 6 is LPC_ADO2, Pin 7 is LPC_ADO3, Pin 8 is LPC_FRAME#, Pin 9 is LPC_ADO, Pin 10 is OVCC3, Pin 11 is LPC_ADO1, Pin 12 is OVCC5, Pin 13 is LPC_ADO2, and Pin 14 is LPC_ADO3. The module is labeled H2X710M-2PITCH_BLACK-RH.

[illegible]

MS-7846

Size Custom	Document Description ATX F_Panel/EMI/TPM	Rev 2.1
Date: Monday, August 12, 2013		Sheet 32 of 38

Reserve debug port 5020



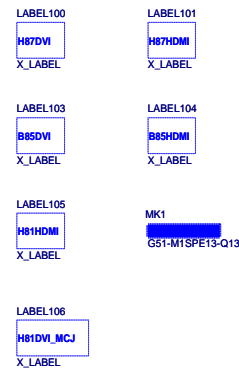
SPI OPT.



CHIPSET OPT.



LABEL OPT.

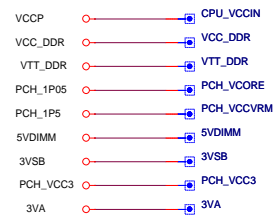
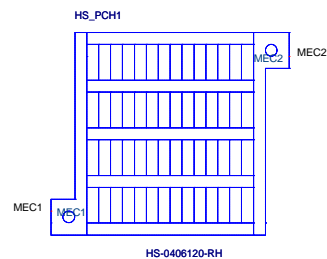


PK0-0784621-G37
PK0-0784621-E48

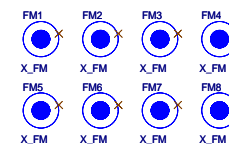
Simulation



PCH XDP PWRGD/RESET



Optical Fiducial Marks-120



Mounting Holes

